**HEWLETT PACKARD**

18 SEGMENT ALPHANUMERIC DISPLAY SYSTEM

HDSP-8716
HDSP-8724
HDSP-8732
HDSP-8740

TECHNICAL DATA   NOVEMBER 1979

Features

- **COMPLETE ALPHANUMERIC DISPLAY SYSTEM UTILIZING THE HDSP-6508 DISPLAY**

- **DISPLAYS 64 CHARACTER ASCII SET**

- **CHOICE OF 16, 24, 32, OR 40 ELEMENT DISPLAY PANEL**

- **MULTIPLE DATA ENTRY FORMATS**
  Left, Right, RAM, or Block Entry

- **EDITING FEATURES THAT INCLUDE CURSOR, BACKSPACE, FORWARDSPACE, INSERT, DELETE, CARRIAGE RETURN, AND CLEAR**

- **DATA OUTPUT CAPABILITY**

- **SINGLE 5.0 VOLT POWER SUPPLY**

- **TTL COMPATIBLE**

- **EASILY INTERFACED TO A KEYBOARD OR A MICROPROCESSOR**
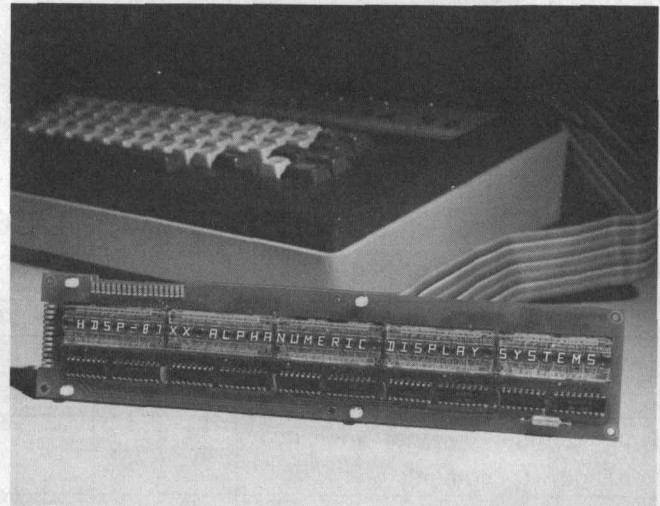
Description

The HDSP-87XX series of alphanumeric display systems provides the user with a completely supported 18 segment display panel. These products free the user's system from display maintenance and minimize the interaction normally required for alphanumeric displays.

Each alphanumeric display system consists of a preprogrammed microprocessor plus associated logic, which provides decode, memory, and drive signals necessary to properly interface a user's system to an HDSP-6508 display. In addition to these basic display support operations, the controller accepts data in any of four data entry formats and incorporates several powerful editing routines. This microprocessor controller is mounted behind a single line display panel consisting of HDSP-6508 displays matched for luminous intensity.

These alphanumeric display systems are attractive for applications such as data entry terminals, instrumentation,, electronic typewriters, and other products which require an easy to use 18 segment alphanumeric display system.

Part Number	Description
HDSP-8716	Single-line 16 Character Alphanumeric Display System utilizing the HDSP-6508 Display
HDSP-8724	Single-line 24 Character Alphanumeric Display System utilizing the HDSP-6508 Display
HDSP-8732	Single-line 32 Character Alphanumeric Display System utilizing the HDSP-6508 Display
HDSP-8740	Single-line 40 Character Alphanumeric Display System utilizing the HDSP-6508 Display

HDSP-8716/-8724/-8732/-8740

Absolute Maximum Ratings

V_{CC} .... -0.5V to 6.0V

Operating Temperature Range,
  Ambient (T_A) .... 0°C to 70°C

Storage Temperature Range (T_S) ...... -40°C to 85°C

Voltage Applied to any
  Input or Output .... -0.5V to 6.0V

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Data Out, Data Valid Ready, Refresh	I_{OL}		3.2	mA
	I_{OH}		-80	μA
Active, Clock	I_{OL}		1.6	mA
	I_{OH}		-40	μA

Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified)

Parameter		Symbol	Min.	Typ.[5]	Max.	Units	Conditions
Supply Current	HDSP-8716/-8724	I_{CC}		560	1150	mA	V_{CC}=5.25V, "$" Displayed in All
	HDSP-8732/-8740	I_{CC}		700	1320	mA	Character Locations, All Outputs Open
Time Average Luminous Intensity Per Digit, 10 Segments on[1]		I_V	.24	.70		mcd	V_{CC}=5.0V, Digit Average '$' Displayed In All Character Locations, T_A=25°C
Input Threshold High (except Reset)		V_{IH}	2.0			V	
Input Threshold High — Reset[2]		V_{IH}	3.0			V	V_{CC}=5.0V ± .25V
Input Threshold Low — All Inputs		V_{IL}			0.8	V	
Data Out, Data Valid, Ready, Refresh, Output Voltage		V_{OH}	2.4			V	I_{OH}=-80μA, V_{CC} = 4.75V
		V_{OL}			0.5	V	I_{OL}=3.2 mA, V_{CC}=4.75V
Active, Clock Output Voltage		V_{OH}	2.4			V	I_{OH}=-40μA, V_{CC}=4.75V
		V_{OL}			0.5	V	I_{OL}=1.6mA, V_{CC}=4.75V
Address,[3] Expand, Input Current		I_{IH}			-0.3	mA	V_{IH}=2.4V, V_{CC}=5.25V
		I_{IL}			-0.6	mA	V_{IL}=0.5V, V_{CC}=5.25V
Blank Input Current		I_{IH}			-0.5	mA	V_{IH}=2.4V, V_{CC}=5.25V
		I_{IL}			-1.0	mA	V_{IL}=0.5V, V_{CC}=5.25V
Reset Input Current		I_{IH}			-0.5	mA	V_{IH}=3.0V, V_{CC}=5.25V
		I_{IL}			-1.0	mA	V_{IL}=0.5V, V_{CC}=5.25V
Data In, Chip Select, Input Current		I_I	-10		+10	μA	0<V_I<V_{CC}
Peak Wavelength		λ_{PEAK}		655		nm	
Dominant Wavelength[4]		λ_d		640		nm	

NOTES:
1. The luminous intensity ratio between segments within a digit is designed so that each segment will have the same luminous sterance. Thus, each segment will appear with equal brightness to the eye.
2. External reset may be initiated by grounding Reset with either a switch or open collector TTL gate for a minimum time of 50ms. For Power On Reset to function properly, V_{CC} power supply should turn on at a rate > 100V/S.
3. Momentary peak surge currents may exist on these lines. However, these momentary currents will not interfere with proper operation of the HDSP-8716/-8724/-8732/-8740.
4. The dominant wavelength, λ_d, is derived from the C.I.E. chromaticity diagram and represents that single wavelength which defines the color of the device, standard red.
5. All typical values at V_{CC} = 5.0V and T_A = 25°C unless otherwise noted.

System Overview

The HDSP-8716/-8724/-8732/-8740 Alphanumeric Display Controllers provide the interface between any ASCII based Alphanumeric System and the HDSP-6508 Alphanumeric Display. ASCII data is loaded into the system by means of any one of four data entry modes — Left, Right, RAM, or Block Entry. This ASCII data is stored in the internal RAM memory of the system. The system may also be expanded to form multiple line panels with system to system control signals.

The user interfaces to any of the system through eight DATA IN inputs, six ADDRESS inputs (RAM mode), a CHIP SELECT input, RESET input, BLANK input, EXPAND input, six DATA OUT outputs, a READY output, DATA VALID output, REFRESH output, and CLOCK output. A low level on the RESET input clears the display and initializes the system. A low level on the CHIP

SELECT input causes the system to load data from the DATA IN and ADDRESS inputs into the system. A special control word causes the controller to output a STATUS WORD, CURSOR ADDRESS, and a string of ASCII characters through the DATA OUT outputs and DATA VALID output. A low level on the EXPAND input allows two or more systems to be configured for multiple line display panels. Pulse width modulation of display luminous intensity can be provided by connecting REFRESH to the input of a monostable multivibrator and the output of the monostable multivibrator to the BLANK input. A 400kHz clock is provided on the CLOCK output. A system block diagram for the HDSP-8716/-8724/-8732/-8740 systems is shown in Figure 1. The system is designed to refresh the display at a fixed refresh rate of 100Hz. The display duty factor is optimized for each display length in order to maximize light output.
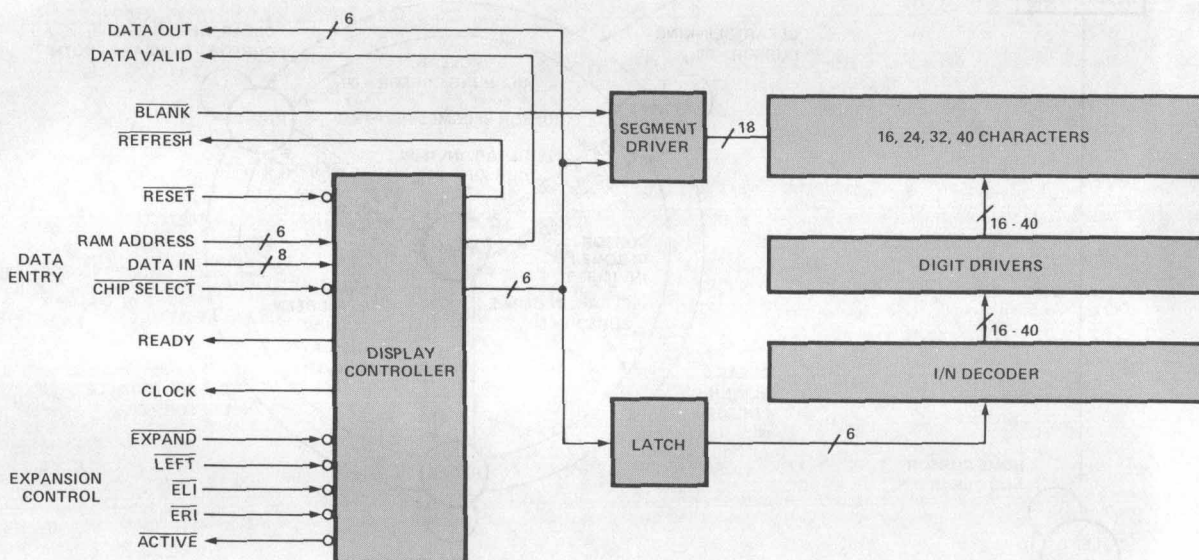

Figure 1. Block Diagram of the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.

Control Mode/Data Entry

User interface to the HDSP-87XX series controller is via an 8-bit word which provides to the controller either a control word or standard ASCII data input. In addition to this user provided 8-bit word, two additional control lines, CHIP SELECT and READY, allow easily generated "handshake" signals for interface purposes.

A logic low applied to the CHIP SELECT input (minimum six microseconds) causes the controller to read the 8 DATA IN lines and determine whether a control word or ASCII data word is present, as determined by the logic state of the most significant bit (D_7). If the controller detects a logic high at D_7, the state of D_6-D_0 will define the data entry mode and appropriate display length.

The 8 bit control data word format is outlined in Figure 2. For the control word (D_7 high), bits D_5 and D_4 define the selected data entry mode (Left entry, Right entry, etc.) and bits D_3 to D_0 define display length. Bit D_6 is ignored.

Control word inputs are first checked to verify that the control word is valid. If the word is valid, the present state — next state table shown in Figure 3 is utilized to determine whether or not to clear the display. RAM entry can be used as a powerful editing tool or can be used to preload the cursor. With other transitions, the internal memory is cleared. The CONTROL WORD $1XXX11XX_2$ is used by the controller to initiate the DATA OUT function.

3

DATA ENTRY CONTROL WORD: $D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0$

1	–	X	X	Y	Y	Y	Y

X	X	DATA ENTRY MODES	Y	Y	Y	Y	DISPLAY LENGTH	
0	0	RAM DATA ENTRY	0	0	1	1	16 DIGITS	HDSP-8716
0	1	LEFT DATA ENTRY	0	1	0	1	24 DIGITS	HDSP-8724
1	0	RIGHT DATA ENTRY	0	1	1	1	32 DIGITS	HDSP-8732
1	1	BLOCK DATA ENTRY	1	0	0	1	40 DIGITS	HDSP-8740

DATA OUT CONTROL WORD: $D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0$

1	–	–	–	1	1	–	–

DATA OUT

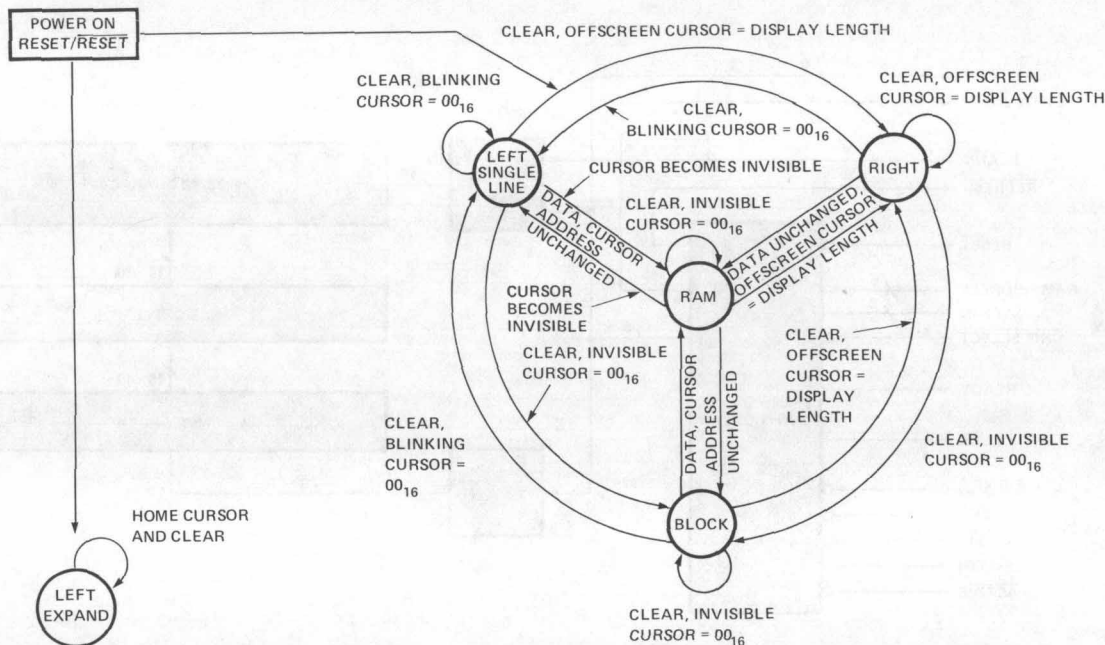**Figure 2. Control Word Format for the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.**

Figure 3. Present State-Next State Diagram for the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.

DATA WORD: $D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0$

0	X	X	X	X	X	X	X

| 0 0 0 1 0 0 0 | BACKSPACE |
0 0 0 1 0 1 0	CLEAR (NEW LINE*)
0 0 0 1 0 0 1	FORWARDSPACE
0 0 0 1 1 0 1	CARRIAGE RETURN
0 0 0 1 1 1 1	INSERT CHARACTER
1 1 1 1 1 1 1	DELETE CHARACTER
0 0 0 1 0 1 1	CURSOR DOWN
0 0 0 1 1 0 0	HOME & CLEAR
0 0 1 1 1 1 0	CURSOR UP

OTHERWISE, THE 7 BIT ASCII CODE

Figure 4. Display Commands for the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.

If D_7 is a logic low when the DATA IN lines are read, the controller will interpret D_6-D_0 as standard ASCII data to be stored, decoded, and displayed. The system accepts the standard 7-bit ASCII code. However, the HDSP-87XX system displays only the 64 character subset $|20_{16}$ (space) to $5F_{16}$ (↑)| and ignores all ASCII characters outside this subset with the exception of those characters defined as display commands. These display commands are shown in Figure 4. The displayed character set for the HDSP-87XX system is shown in Figure 5.

Regardless of whether a control word or ASCII data word is presented by the user, a READY signal is generated by the controller after the input word is processed. This READY signal goes low for $35\mu s$ and upon a positive transition, a new $\overline{\text{CHIP SELECT}}$ may be accepted by the controller. Data Entry Timing is shown in Figure 6.

BITS	D_3 D_2 D_1 D_0	0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 0 1 0	1 0 1 1	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1
D_6 D_5 D_4	HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 1 0	2	(space)	!	''	‡	$	%	&	'	⟨	⟩	*	+	,	−	.	/
0 1 1	3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
1 0 0	4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
1 0 1	5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	↑	←

Figure 5. Display Font for the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.
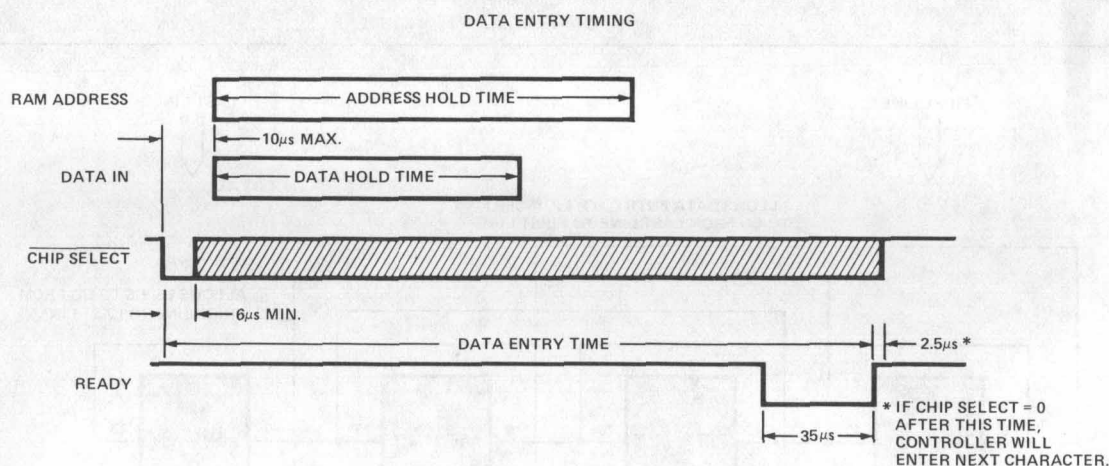
DATA ENTRY TIMING

MAXIMUM DATA ENTRY TIMES OVER OPERATING TEMPERATURE RANGE

DATA ENTRY MODE		FUNCTION										
	DATA HOLD TIME*	DATA ENTRY	BS	HT	LF	CR	US	INSERT	DEL	VT	FF	RS
LEFT, SINGLE	$25\mu s$		$250\mu s$	$215\mu s$	$235\mu s$	$505\mu s$	$220\mu s$	$200\mu s$	$665\mu s$	$645\mu s$		
LEFT, EXPANDED	$25\mu s$		$345\mu s$	$265\mu s$	$265\mu s$	$265\mu s$	$245\mu s$	$245\mu s$	$705\mu s$	$690\mu s$	$250\mu s$	$530\mu s$	$245\mu s$
RIGHT	$25\mu s$		$480\mu s$	$480\mu s$		$485\mu s$						
RAM	$25\mu s$ $145\mu s$**		$220\mu s$									
BLOCK	$25\mu s$		$130\mu s$ (165μs FOLLOWING RIGHTMOST CHARACTER)									
CONTROL	$25\mu s$		$545\mu s$									
DATA OUT	$25\mu s$		$280\mu s + 36n\mu s$, WHERE n = CONFIGURED DISPLAY LENGTH									

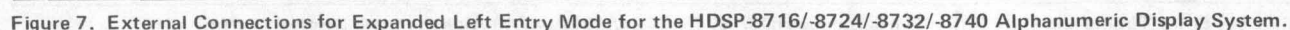*MINIMUM TIME THAT DATA INPUTS MUST REMAIN VALID AFTER CHIP SELECT GOES LOW.
**MINIMUM TIME THAT RAM ADDRESS INPUTS MUST REMAIN VALID AFTER CHIP SELECT GOES LOW.

Figure 6. Data Entry Timing and Data Entry Times for the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.

5

Left Entry Mode

With Left entry, characters are entered in typewriter fashion, i.e., to the right of all previous characters. Left entry uses a blinking cursor to indicate the location where the next character is to be entered. CLEAR loads the display with spaces and resets the cursor to the leftmost display location. BACKSPACE and FORWARDSPACE move the cursor without changing the character string. Thus, the user can backspace to the character to be edited, enter a character and then forwardspace the cursor. CARRIAGE RETURN resets the cursor to the leftmost display location leaving the display unchanged. The DELETE function deletes the displayed character at the cursor location and then shifts the character string following the cursor one location to the left to fill the void of the deleted character. The INSERT CHARACTER sets a flag inside the system that causes subsequent ASCII characters to be inserted to the left of the character at the cursor location. As new characters are entered, the cursor, the character at the cursor, and all characters to the right of the cursor are shifted one location to the right. The INSERT function is terminated by a second INSERT CHARACTER, or by BACKSPACE, FORWARDSPACE, CLEAR, CARRIAGE RETURN, or DELETE. In Left entry mode, after the display is filled, the system ignores all characters except BACKSPACE, CARRIAGE RETURN, and CLEAR. The system allows the cursor to be positioned only in the region between the leftmost display character and immediately to the right (offscreen) of the rightmost display character.

Expanded Left entry is selected by grounding the EXPAND input prior to RESET. Expanded Left entry mode allows several HDSP-87XX systems to be connected into a multiple line panel. Expanded Left entry uses the ERI input, ELI input, LEFT input, and ACTIVE output to provide a handshake between each system as shown in Figure 7. With the proper connections, the cursor can be moved in a circular fashion from the end of the last line to the beginning of the first line, or such that it shifts offscreen and is lost until the next CLEAR/HOME display command. Expanded Left entry adds three display commands: CURSOR UP moves the cursor to the same location in the preceeding line; CURSOR DOWN moves the cursor to the same location in the following line; CLEAR/HOME loads all displays with spaces and resets the cursor to the leftmost display location in the first line. The CLEAR command in Left entry mode is replaced by the LINE FEED function. LINE FEED moves the cursor to the leftmost display location in the following line leaving the current line unchanged.

Right Entry Mode

In Right entry mode, characters are entered at the right hand side of the display and shifted to the left as new characters are entered. In this mode, the system stores 48 ASCII characters, although only the last characters entered are displayed. CLEAR loads the display with spaces. BACKSPACE shifts the display one location to the right, deleting the last character entered and displaying the next character in the 48 character buffer. Right entry mode is a simple means to implement the walking or "Times-Square" display. In this mode, the cursor is located immediately to the right (offscreen) of the rightmost displayed character.

Figure 7. External Connections for Expanded Left Entry Mode for the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.

6

Block Entry Mode

Block entry allows the fastest data entry rate of all four modes. In this mode, characters are loaded from left to right as with Left entry. However, with Block entry, after the display is completely loaded, the next ASCII character is loaded in the leftmost display location, replacing the previous displayed character. While Block entry has a non-visible cursor, the cursor is always loaded with the address of the next character to be entered. The display can be cleared and the cursor reset to the leftmost display location by loading in a new BLOCK control word.

RAM Entry Mode

In RAM entry, ASCII characters are loaded at the address specified by the six bit RAM address. Regardless of display length, address 00 is the leftmost display character. Out of range RAM addresses are ignored. While RAM entry has a non-visible cursor, the cursor is always preloaded with the address to the right of the last character entered. This allows the cursor to be preloaded with an address prior to going into any other entry mode. The display can be cleared by loading in a new RAM control word.

Power-On Reset/Reset

When power is first applied to the system, the system clears the display and tests the state of the DATA INPUT, D_7. If $D_7 > 2.0V$, the system loads the control word on the DATA INPUTS into the system. If $D_7 \leq 0.8V$ or the system sees an invalid control word, the system initializes as Left entry for a 40 character display with a flashing cursor in the leftmost location. During $\overline{RESET}$, the system also tests the state of the $\overline{EXPAND}$ input. If $\overline{EXPAND}$ is low, the system initializes in expanded left entry mode. A flow chart that describes the $\overline{RESET}$ function is shown in Figure 8. For POWER-ON RESET to function properly, the
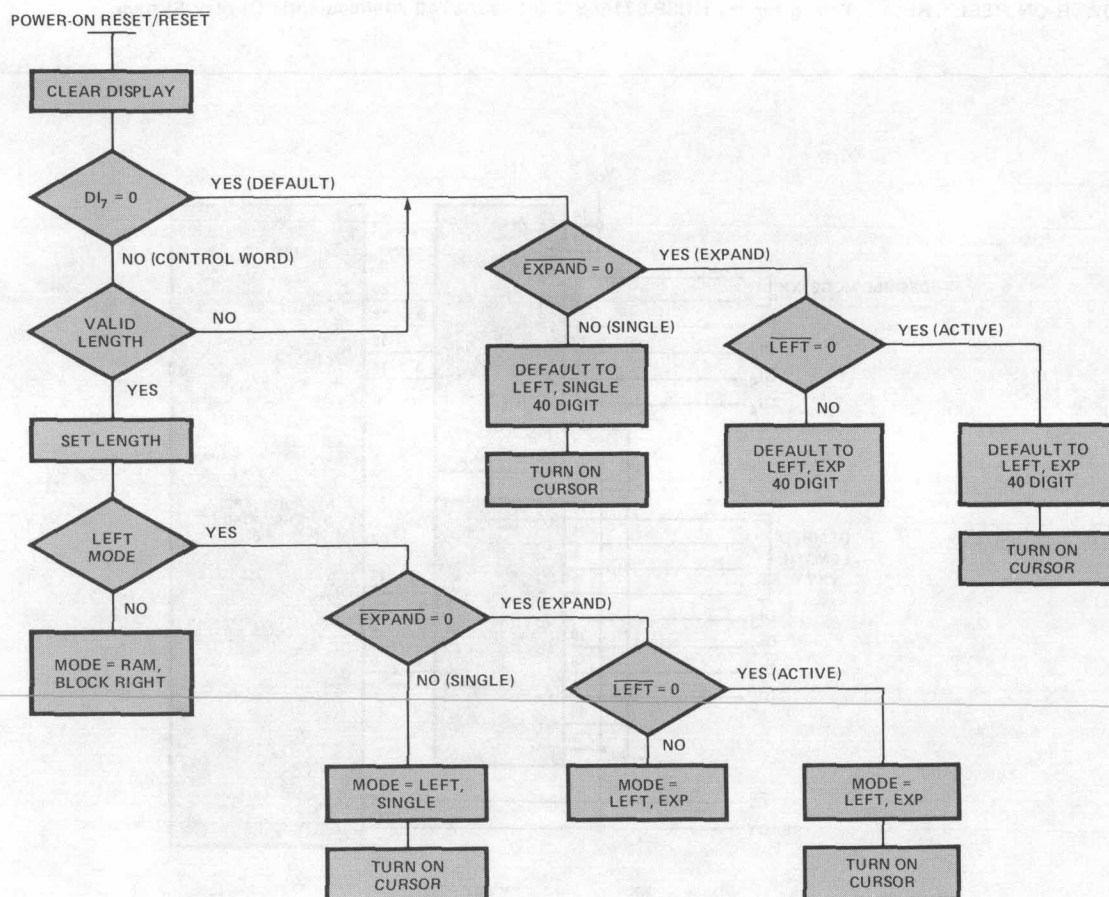

Figure 8. Reset Sequence for the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.

7

power supply must turn on at a rate > 100 V/s. In addition, the system can be reset by pulling the $\overline{\text{RESET}}$ input low for a minimum of 50 milliseconds. POWER-ON RESET/$\overline{\text{RESET}}$ timing is shown in Figure 9.

If some entry mode or display length is desired other than 40 character Left entry, it is necessary to either load the appropriate control word or provide a control word during POWER-ON RESET/$\overline{\text{RESET}}$. The circuit shown in Figure 10 can be used to load any desired preprogrammed control word into the HDSP-87XX Series Display Controller during POWER-ON RESET/$\overline{\text{RESET}}$.
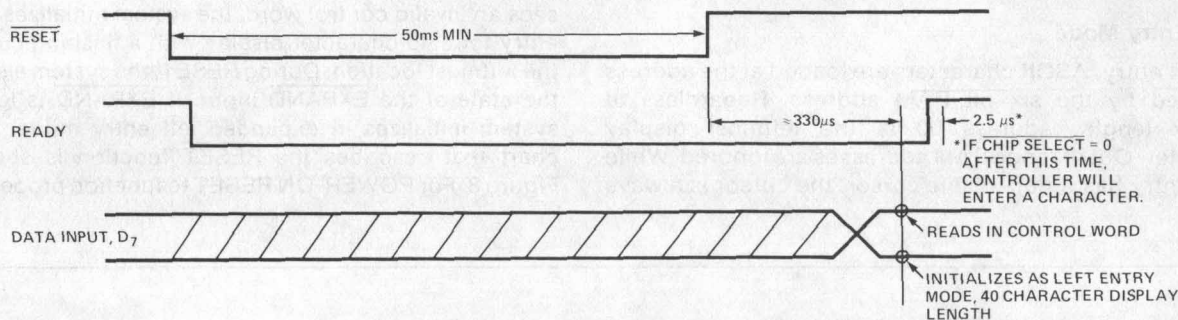
Figure 9. POWER-ON RESET/$\overline{\text{RESET}}$ Timing for the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.

XX		YYYY	
00	RAM	0011	16 DIGITS
01	LEFT	0101	24 DIGITS
10	RIGHT	0111	32 DIGITS
11	BLOCK	1001	40 DIGITS
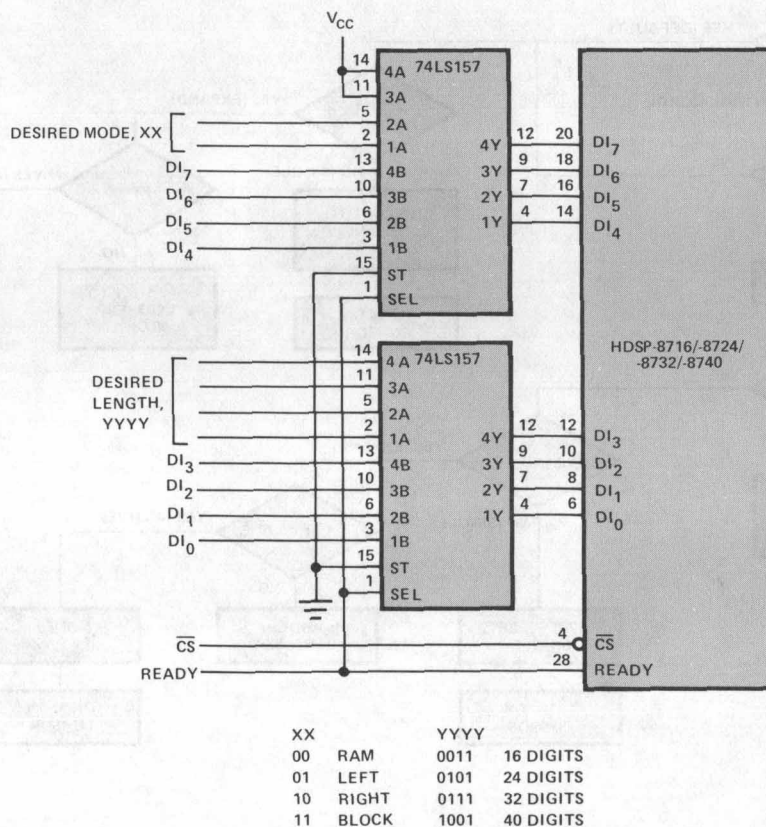
Figure 10. External Circuitry to Load a Control Word into the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System Upon POWER-ON RESET/$\overline{\text{RESET}}$.

Data Out

Data stored in the HDSP-87XX system is available to the user upon command. Data Out is initiated by the control word $1XXX11XX_2$. Following this control word, the system outputs a STATUS WORD, CURSOR ADDRESS, and a string of ASCII data characters. The STATUS WORD specifies the data entry mode and the display length of the system. The STATUS WORD is the same format as a valid control word with D_7 and D_6 deleted. The CURSOR ADDRESS specifies the location of the cursor within the display. The CURSOR ADDRESS of the leftmost display location is address 00. In Expanded Left entry mode, a CURSOR ADDRESS of 63 ($3F_{16}$) is used to indicate a non-active line. The system outputs the same number of ASCII data characters as the display length specified by the control word. The first ASCII data character is always the leftmost display character. The positive edge of the DATA VALID output can be used to load the DATA OUTPUT words into the user's system. The DATA OUT timing for the HDSP-87XX systems is summarized in Figure 11.

Luminous Intensity Modulation

Pulse width modulation of display luminous intensity can be provided by connecting the REFRESH output of the system to the input of a monostable multivibrator. The output of the monostable multivibrator should then be connected to the BLANK input of the system. Modulation of display luminous intensity is then achieved by varying the delay of the monostable multivibrator with a potentiometer or photoresistor. REFRESH is repeated at a rate of 10ms divided by the configured display length. For example, an HDSP-8732 system, when configured for a 32 character display length, would pulse the REFRESH output every 312.5µs. The circuit shown in Figure 12 may be utilized to provide manual control of display luminous intensity. Automatic control may be achieved by substituting an appropriate value photoconductor for potentiometer R_1. If luminous intensity modulation is not desired, BLANK should be left open.
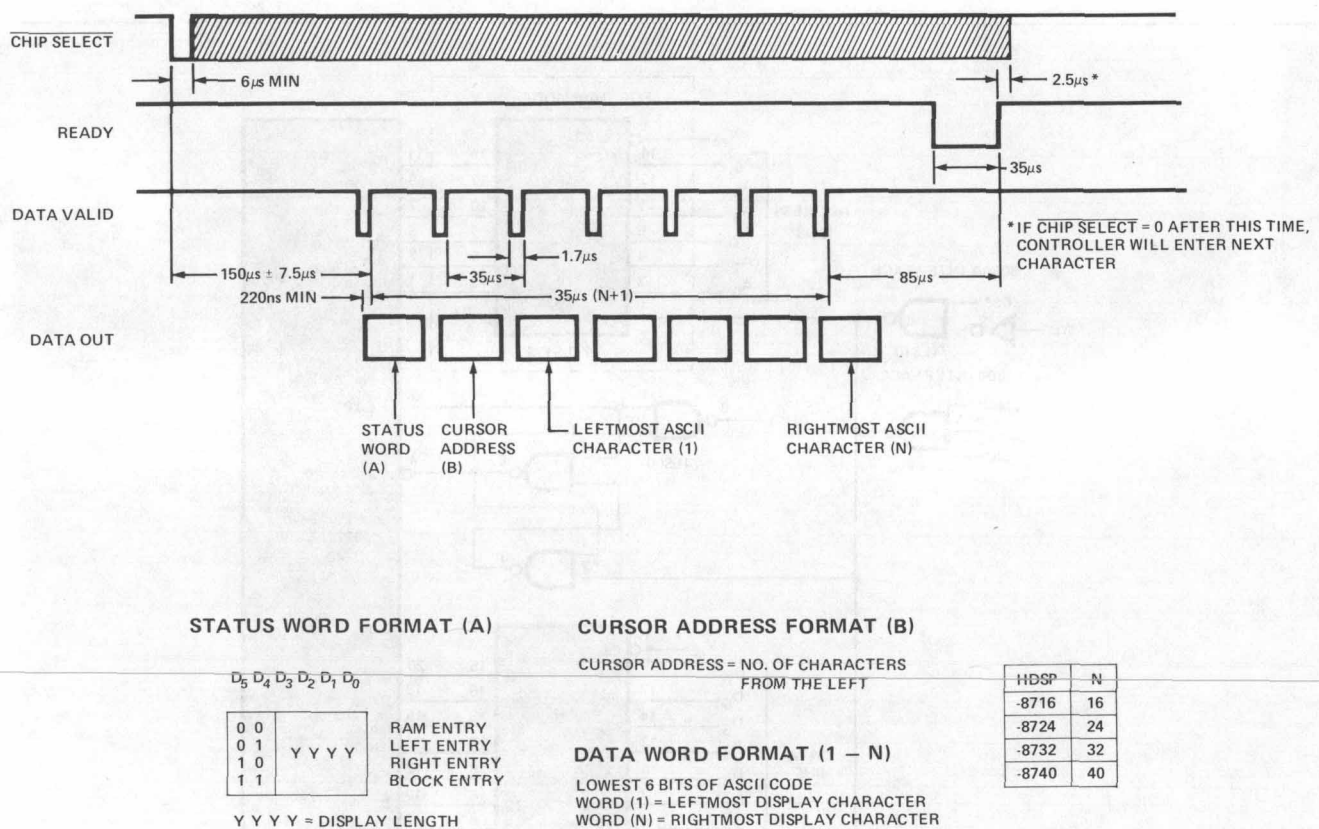

HDSP	N
-8716	16
-8724	24
-8732	32
-8740	40

STATUS WORD FORMAT (A)

$D_5 D_4 D_3 D_2 D_1 D_0$

0 0		RAM ENTRY
0 1	Y Y Y Y	LEFT ENTRY
1 0		RIGHT ENTRY
1 1		BLOCK ENTRY

Y Y Y Y = DISPLAY LENGTH

CURSOR ADDRESS FORMAT (B)

CURSOR ADDRESS = NO. OF CHARACTERS FROM THE LEFT

DATA WORD FORMAT (1 – N)

LOWEST 6 BITS OF ASCII CODE
WORD (1) = LEFTMOST DISPLAY CHARACTER
WORD (N) = RIGHTMOST DISPLAY CHARACTER

Figure 11. Data Out Timing and Format for the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.

Microprocessor Interface

Interfacing the HDSP-87XX Series Display System to microprocessor systems depends on the needs of the particular application. Figure 13 shows a latched interface between the host microprocessor and the HDSP-87XX system. The latch provides temporary storage to avoid making the host microprocessor wait for the system to accept data. Data from the host microprocessor system is loaded into the 74LS273 octal register on the positive transition of the clock input (pin 11). At the same time, the CHIP SELECT input is forced low. The CHIP SELECT input stays low until READY goes low. The host microprocessor should avoid loading new data into the 74LS273 as long as BUSY is high. The latched interface can be implemented with an octal register and $\overline{SR}$ flip-flop if the HDSP-87XX system is operated in Left, Right, or Block entry. RAM entry requires an additional register for the RAM address inputs. Additional flexibility can be achieved by using a peripheral interface adapter (PIA) to interface the HDSP-87XX system to the host microprocessor system. The PIA provides a data entry handshake between the host microprocessor system and the HDSP-87XX system and allows the host microprocessor system to read the Data Output port of the HDSP-87XX system.
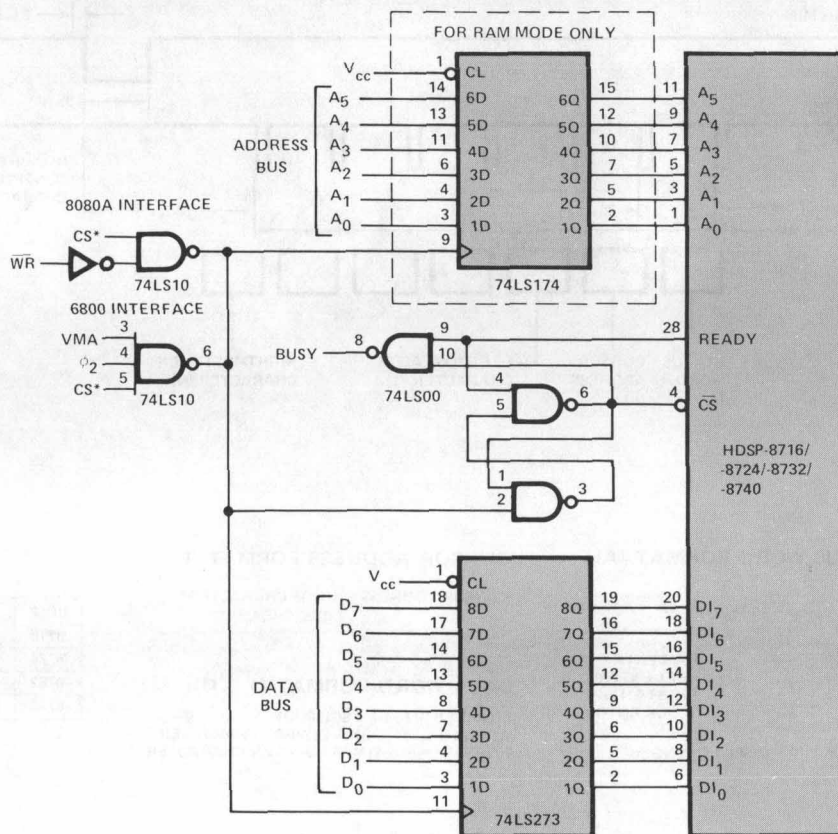
C = .033µF   HDSP-8716
C = .022µF   HDSP-8724
C = .015µF   HDSP-8732/-8740
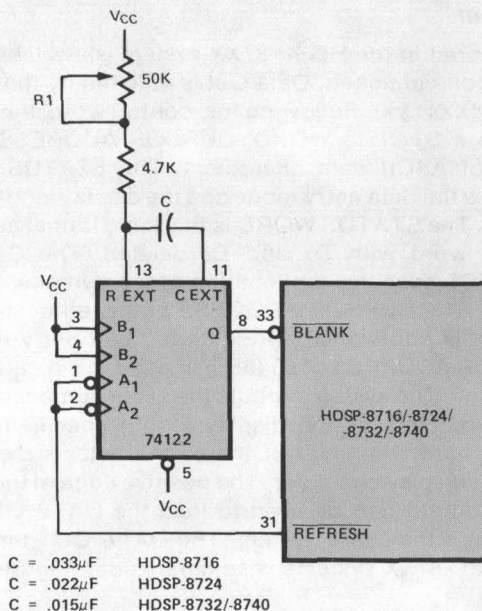
Figure 12. External Circuitry to Vary the Luminous Intensity of the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.
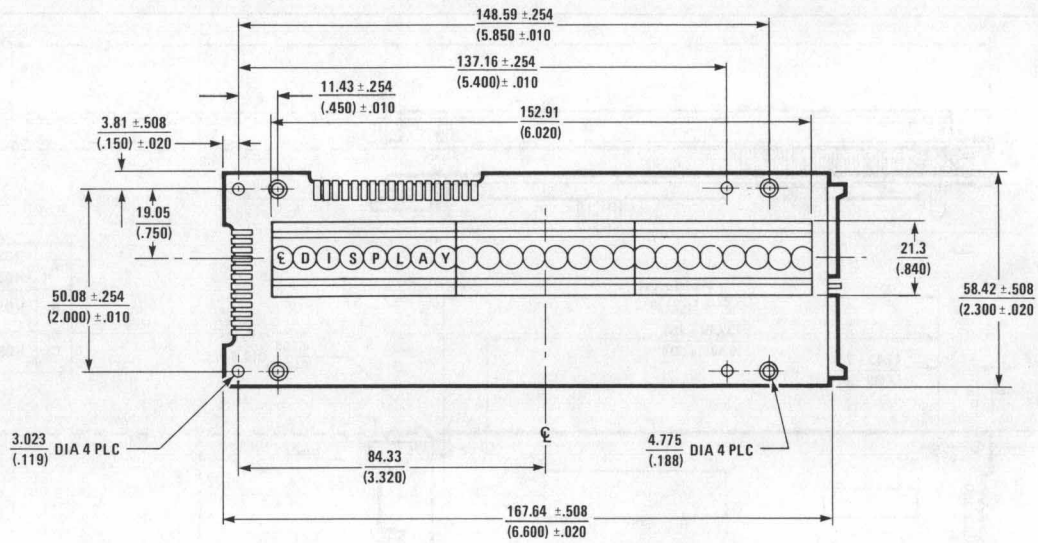
*CS IS A LOGICAL COMBINATION OF HIGH ORDER ADDRESS BITS THAT DISTINGUISH THE ADDRESS OF THE HDSP-8716/-8724/-8732/-8740 FROM THE REST OF THE MICROPROCESSOR SYSTEM.

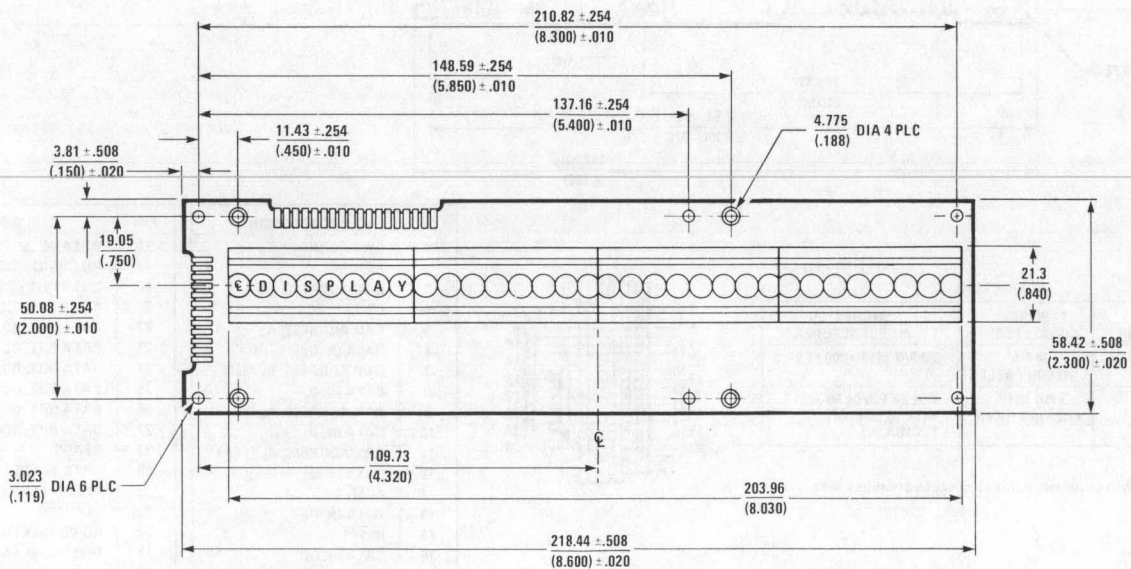**Figure 13. Latched Interface to the HDSP-87XX Series Alphanumeric Display System.**
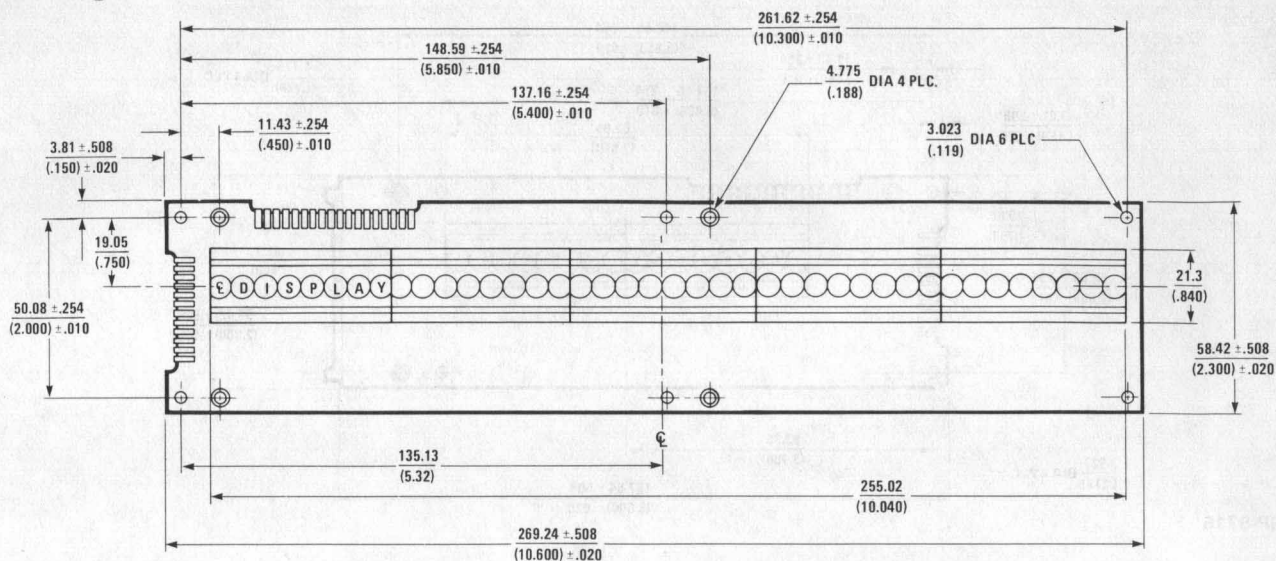
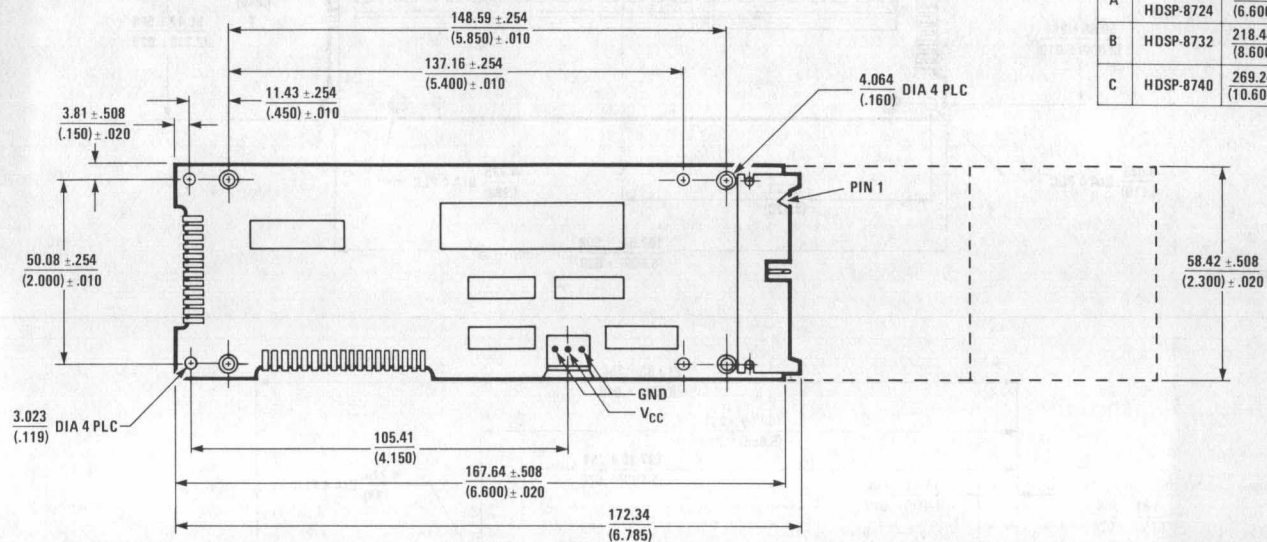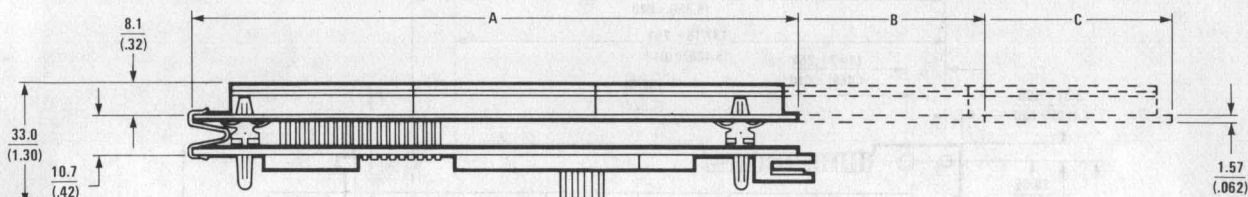# Package Dimensions


HDSP-8716

HDSP-8724

HDSP-8732

11
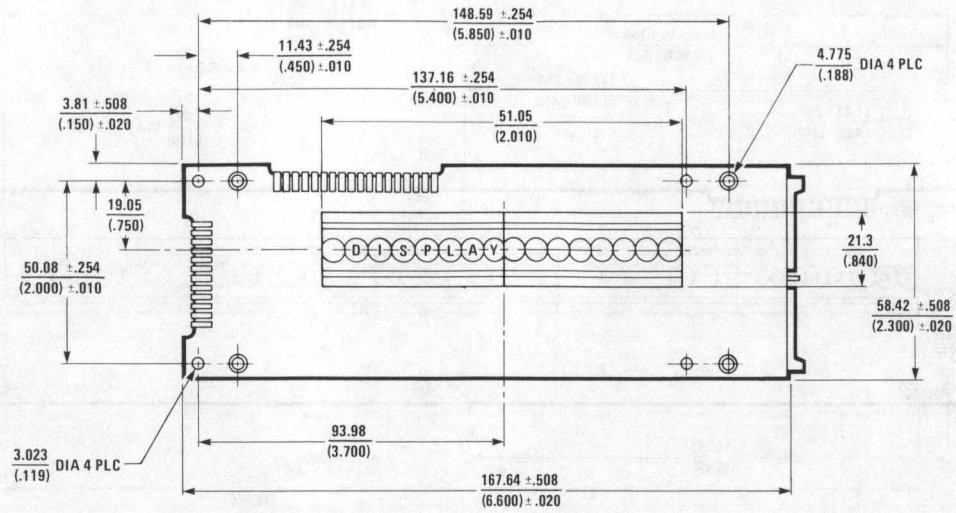
Package Dimensions

HDSP-8740

A	HDSP-8716 HDSP-8724	167.64 (6.600)
B	HDSP-8732	218.44 (8.600)
C	HDSP-8740	269.24 (10.600)

PIN 1

GND
V_CC

HDSP-8716/-8724/-8732/-8740

CONNECTORS

FUNCTION	TYPE OF CONNECTOR	SUGGESTED MANUFACTURER
CONTROL/DATA ENTRY	34 PIN RIBBON CABLE	3M P/N 3414-X000 SERIES
POWER(1)	3 PIN WITH LOCKING RAMP	MOLEX P/N 09-50-3031 WITH 08-50-0106 TERMINALS

NOTES: (1) POWER LEADS SHOULD BE 18-20 GAUGE STRANDED WIRE.
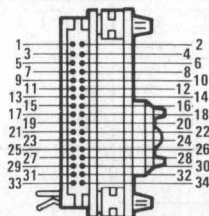
PIN	DESCRIPTION
1	RAM ADDRESS, A_0
2	EXPAND
3	RAM ADDRESS, A_1
4	CHIP SELECT
5	RAM ADDRESS, A_2
6	DATA IN, D_0
7	RAM ADDRESS, A_3 (ELI)
8	DATA IN, D_1
9	RAM ADDRESS, A_4 (ERI)
10	DATA IN, D_2
11	RAM ADDRESS, A_5 (LEFT)
12	DATA IN, D_3
13	ACTIVE
14	DATA IN, D_4
15	RESET
16	DATA IN, D_5
17	NO CONNECTION

PIN	DESCRIPTION
18	DATA IN, D_6
19	NO CONNECTION
20	DATA IN, D_7
21	NO CONNECTION
22	DATA OUT, DO_0
23	DATA OUT, DO_1
24	DATA OUT, DO_2
25	DATA OUT, DO_3
26	DATA OUT, DO_4
27	DATA OUT, DO_5
28	READY
29	DATA VALID
30	400 kHz CLOCK OUT
31	REFRESH
32	NO CONNECTION
33	DISPLAY BLANK
34	NO CONNECTION