3450A Multifunction DVM

TROUBLESHOOTING GUIDE

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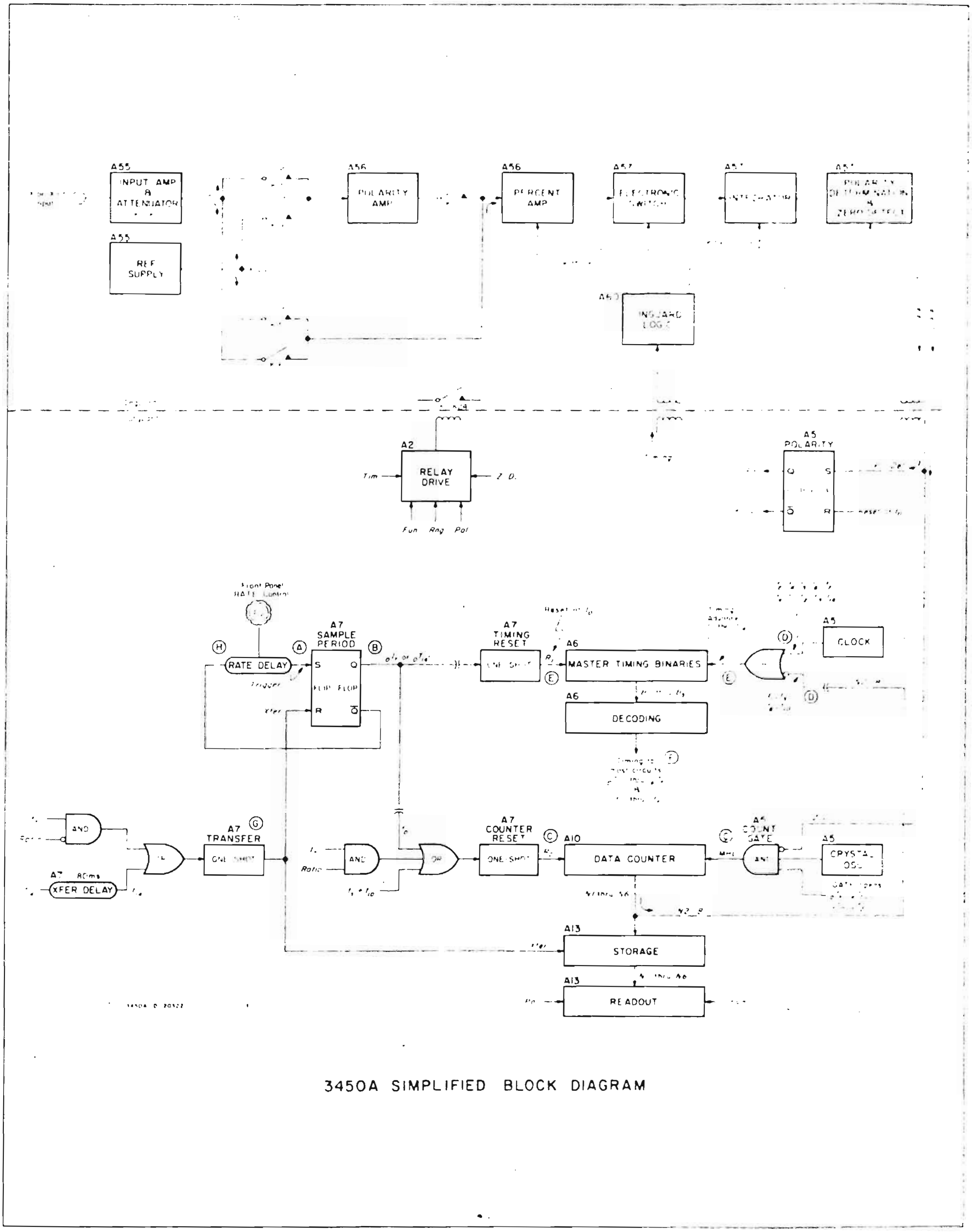
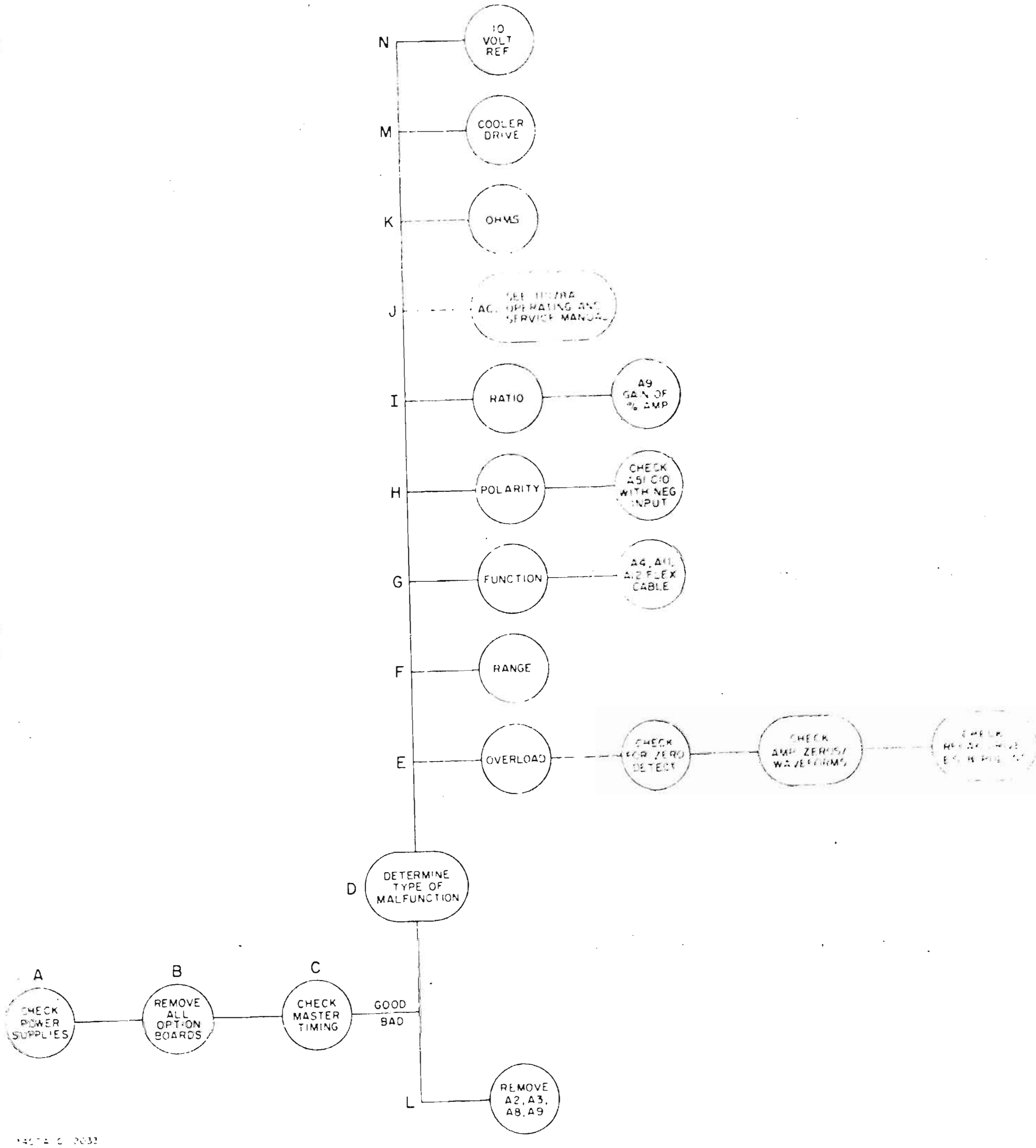


3450A SIMPLIFIED BLOCK DIAGRAM



Troubleshooting Tree

A. Check Power Supplies. The 3450A power supply system is divided into two sections: 1) the inguard supplies which use the inguard ground as a reference; and 2) the outguard supplies which use the chassis as a reference. There is nothing really unique about the power supply circuits that would require any special troubleshooting techniques. Troubleshooting is largely a matter of finding the right circuit board and knowing where the various supplies are used. Table 1 given on the next page will provide the basic layout of the power supply system as well as information concerning the location and use of each supply. The Operating and Service Manual provides the adjustment procedure for the outguard +4.4 volt supply and the ±17 volt inguard supply.

B. Remove All Option Boards. The 3450A is basically a 10 volt DVM; the ohms and AC sections are used to convert their input signals to DC levels. The other options control or process the digitized measurement. Since these option boards can be removed conveniently, a problem can be isolated to any of the options or the main frame.

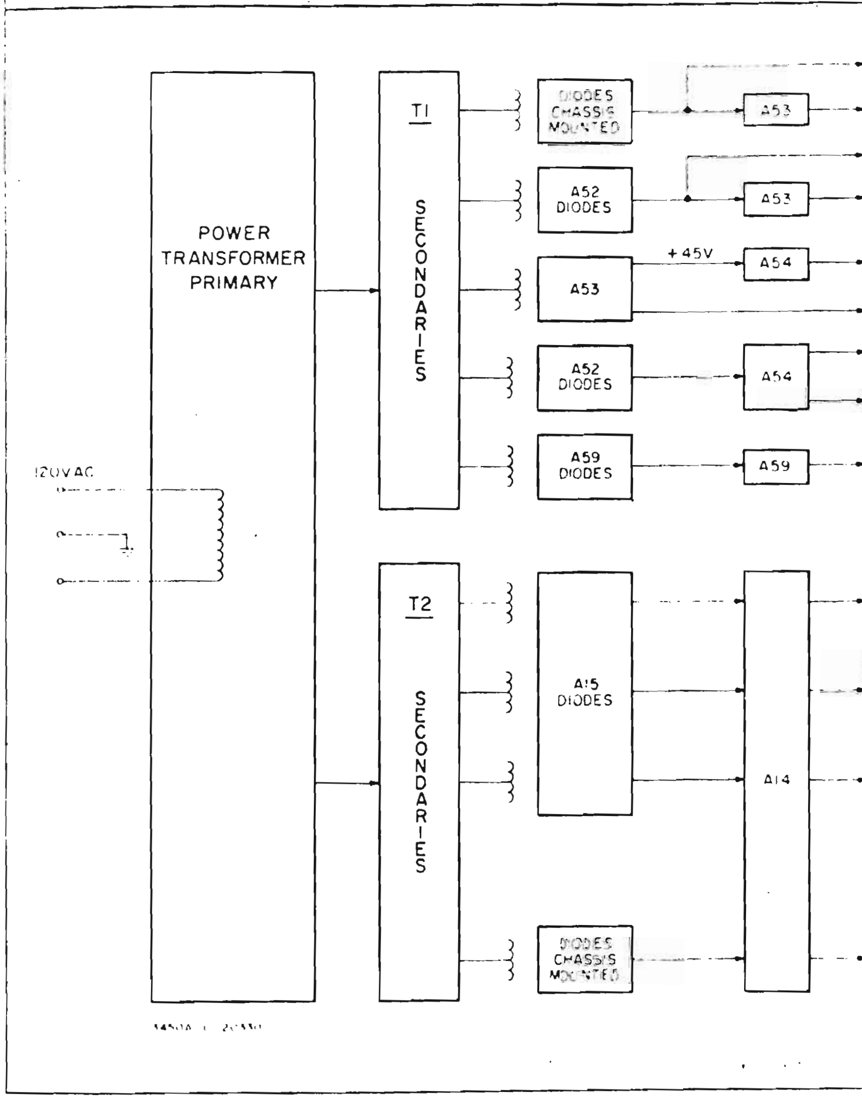
Remove circuit boards A3, A24, A25, the Ohms Coverter, and the AC Converter. Provide a 10 volt DC signal to the 3450A. If the instrument will now function, re-install each option one at a time. After each option has been installed, measure the 10 V DC signal again. This procedure will locate the option that is malfunctioning. Troubleshooting information for the AC Converter is contained in the 11078A Operating and Service Manual. Ohms converter troubleshooting information is contained in this guide.

If the instrument does not operate with all options removed, continue to the next paragraph.

C. The Master Timing Loop. These circuits provide all of the timing signals as well as the actual data counts and readout. A malfunction in this section will likely be apparent from the front panel. The sample rate light and rate control potentiometer will not be functioning properly. Either the sample rate light will be flashing at some odd frequency or the light may not flash at all. Also, the rate control potentiometer may not have any sample rate control.

The Sample Period flip-flop output is available at A7TP1. Trigger an oscilloscope at A6TP6 on the positive slope and observe the sample period waveform. This display is someti difficult to obtain. If the sample rate control potentiometer will adjust the sample rate, then decrease the sample rate. (See Figure 1) If the rate potentiometer has no effect see Figure 2. If the sample rate is being generated but the rate light is not blinking, the fault may be on A11, A12 or the rate light. If the sample period is not present at A7TP1 continue to paragraph L.

BLOCK DIAGRAM OF POWER SUPPLY SYSTEM



[illegible]	[illegible]
+9V ±1.5V	A54
+5V ± 0.5V	A56, A57, A59, A60, A66, A69, A72
-9V ± 1.5V	A54
-5V ±0.5V	A57, A5[illegible], A66, A69
+34V +1.5V -1V	A55, A56, A57
-35V +1V -1.5V	A54, A55, A56, A57
+17V ± 20mV	A53, A55
-17V ± 20mV	A53, A56, A57, A59, A60, A72
+3.09V ± 50mV	A59 (OHMS REFERENCE)
-6.5V ±1V	A14
+200V +50V -10V	A13, A30
+12V ±1V	A3, A5, A6, A24, A25
+4.4V ±75mV	A2, A3, A4, A5, A6, A7, A8, A9, A10, A1[illegible], A17, A24, A25, A30

TABLE 1.

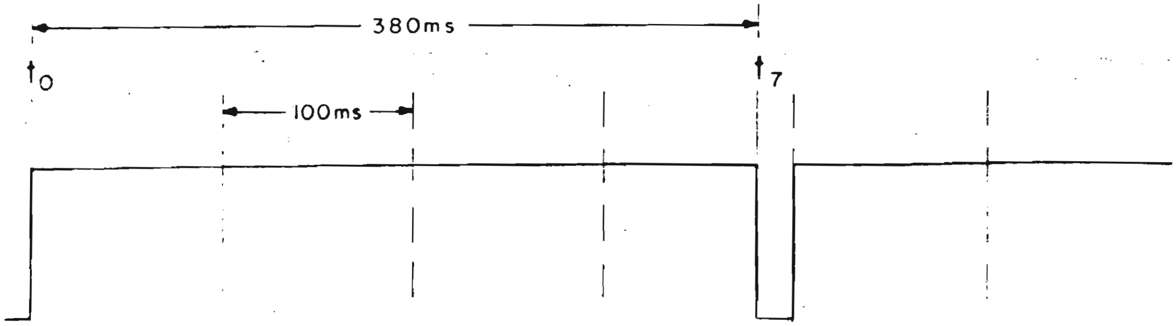


Figure 1. Sample Period with no rate control.

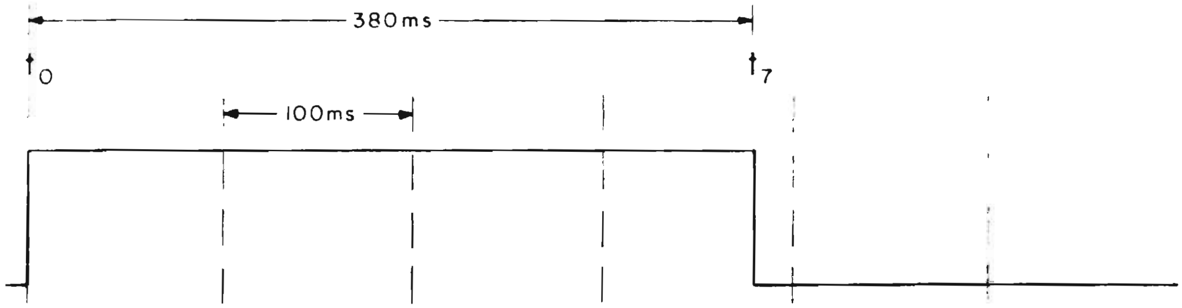


Figure 2. Sample Period with rate control.

D. Determine the Type of Malfunction. Try to determine the general area of the trouble. Refer to the "tree" for the various troubleshooting sections. As an example, if the front panel is indicating overload, proceed to paragraph E.

E. Overload. If the front panel indicates overload, short A6TP2 to A6TP3. This will generate a false zero-detect. If the problem is associated with the analog portion of the instrument, the front panel readout will be approximately 45000 to 50000 counts. If not, proceed to paragraph L or paragraph F.

The purpose of the analog section of the instrument is to generate the zero-detect signal and transmit that signal through the pulse transformer to the timing section.

If this signal is not received, the Data Counters will continue to count until overload is reached. If shorting these two test points, A6TP2 and A6TP3, does provide a zero-detect signal, then either a zero-detect is not being generated or it is not being transmitted from the analog section. Shorting these two test points provides a false zero-detect to the timing section. This signal is at T_5 and is generated by A6IC6.

AMPLIFIER CHECK

The 3450A analog amplifiers must be zeroed. Check the amplifier zeros using the 3450A Operating and Service Manual page 5-8. If these zeros are all okay, check the amplifier waveforms. See Figures 3 and 4. The figures show the various waveforms for both a positive and negative input. If any amplifier will not zero, isolate that amplifier and provide a zero input. For example, if the Polarity Amplifier will not zero, remove A55 and the orange lead to the Percent Amplifier. Short the input of the Polarity Amplifier to inguard ground. If the Polarity Amplifier output will swing from + to -, then check the Input Amplifier and Percent Amplifier. If

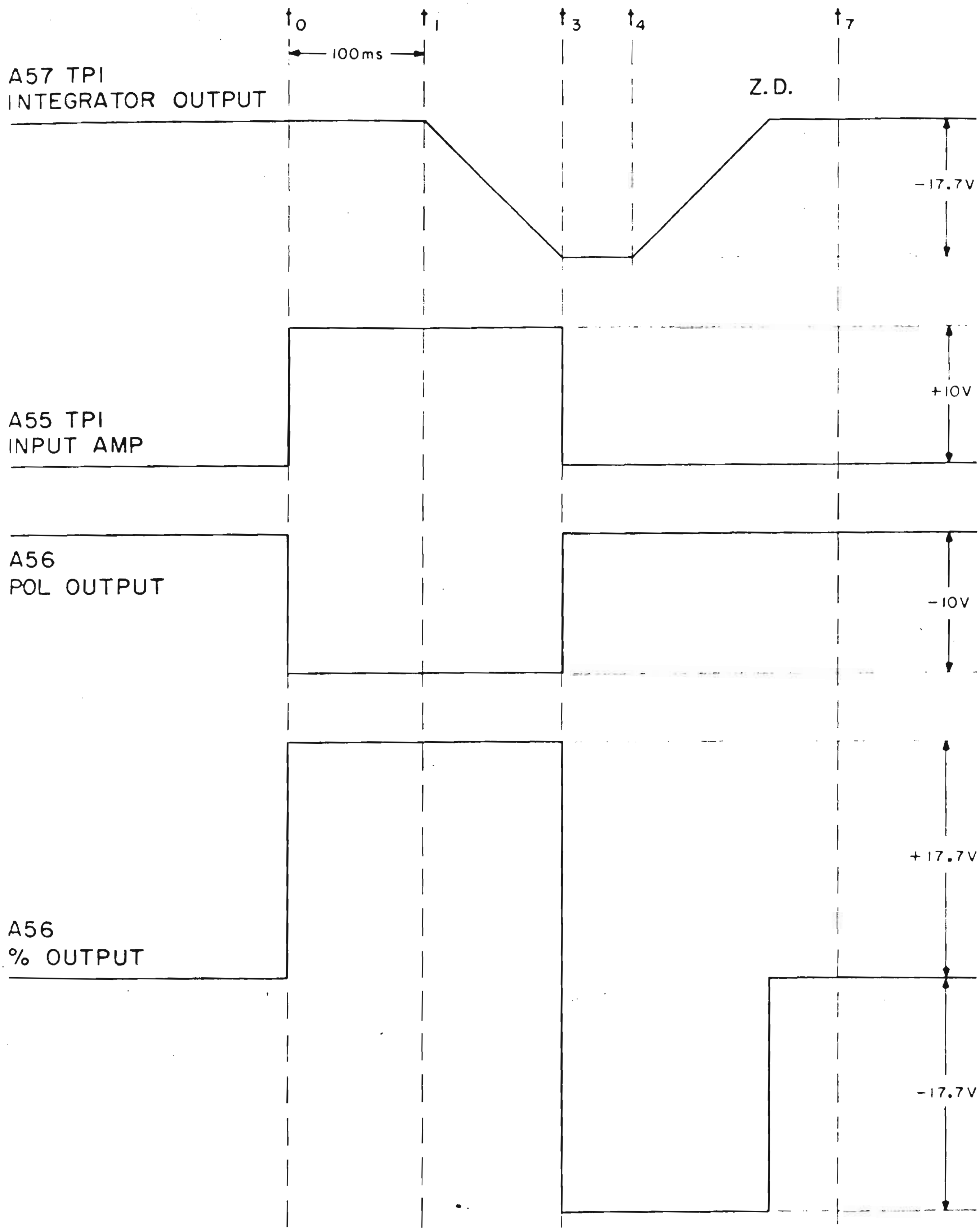


Figure 3. Amplifier Waveforms with positive 10 volt input.

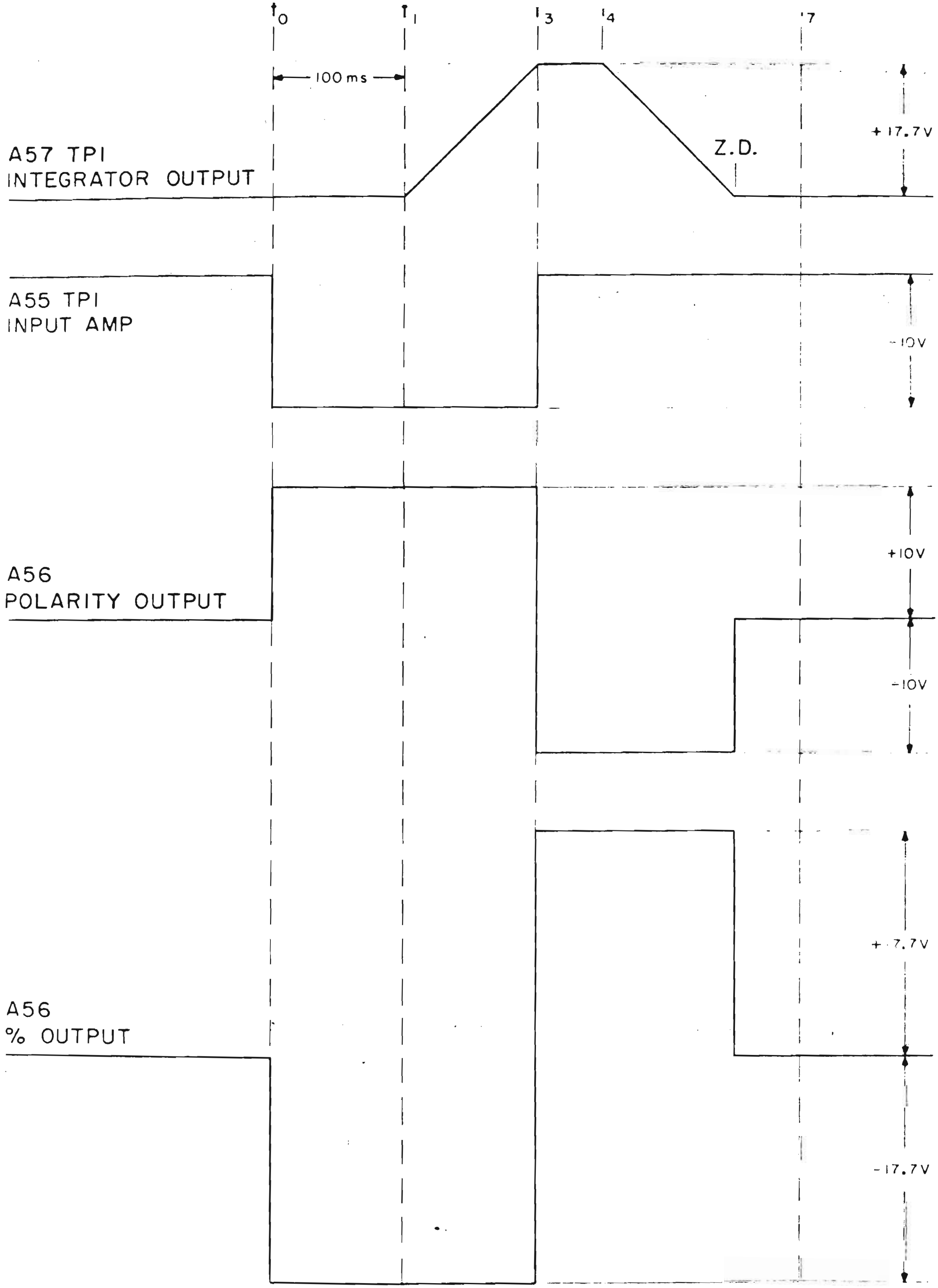


Figure 4. Amplifier Waveforms with negative 10 volt input.

Polarity Amplifier will not zero, it is unbalanced. This condition could be caused by any of several components. However, the input stage of the Polarity Amplifier is a dual-pack FET and is located in the cooler. The big question to be answered now is, "Are the FET's okay?" If so, the repair will proceed fast and easy. Troubleshooting for each Amplifier is contained in the following paragraphs.

Input Amplifier

The input amplifier uses an auto-zero circuit to compensate for small amounts of amplifier offset. This circuit is operated by three reed relays, K7, K8 and K9. If K9 relay is not working, the instrument might read overload. To check this relay, select MAN EXT and short A55TP1 to the K9 side of Auto-Zero capacitor, A70C1. Trigger the instrument and if the front panel indication is no longer overload, the problem is that K9 is not closing. If the instrument does not come out of overload, the relay is probably okay and the problem is in the amplifier.

The next step is to break the feedback loop and operate the amplifier
This is done by removing circuit board A2. Remove the short from A70C1 to A55TP1 and connect a short from the top A70C1 to inguard ground and from the top of A69C1 to inguard ground. Connect an -hp- Model 419A to A55TP1 and inguard ground. Adjusting A55R14, Input Amplifier Zero adjust, the amplifier should swing from positive to negative saturation.

If this is not the case, check the emitter-base voltages of transistors A55Q1, Q2, Q3, Q4 and Q5. When making these voltage checks leave the A2 Assembly out. If these transistors all look good, the problem may be that the input FET's are bad.

Checks for A55Q2 - Q8

A basic in-circuit check for any transistor consists of answering three questions about the transistor: 1) Is the transistor shorted B-E?, 2) Is the transistor open B-E?, and 3) Does the transistor work like a transistor? (i.e. does the base-emitter voltage control the collector voltage.) The 3450A should be in MAN EXT.

1) Base-Emitter Short

Connect an -hp- Model 412A across the base-emitter junction. If this voltage, forward biased, is zero, then transistor could legitimately be turned off. If the emitter base voltage is zero, try to forward bias the emitter-base junction. As an example, if the emitter-base junction of A55Q2 measures zero, short the emitter to base of A55Q1A. This will turn off A55Q1A thereby raising Q1A's collector voltage. If there is still no change in A55Q2 emitter-base voltage then the transistor is shorted.

2) Base-Emitter Open

Connect an -hp- Model 412A across the emitter-base junction. If the forward biased voltage exceeds a value greater than 0.5 to 1.0 volts, the emitter-base junction is open. Again, the transistor may be legitimately turned off (i.e. emitter-base voltage is zero). Therefore, the base voltage should be varied, and compared again with the emitter voltage. If, however, there ever exists an emitter-base forward biased voltage of greater than 1 volt, the transistor is faulty.

There are other transistor failures possible. A couple of these are:

1) Open from collector to emitter and 2) Short from collector to emitter.

Finding either of these failures is quite similar. If the collector voltage is insensitive to base-emitter voltage and remain somewhere close to the power supply, then the fault is a collector-emitter open. If, in the same case, the collector voltage is considerably below the power supply, then the fault is a collector-emitter short.

If all of these transistors check-out then the problem is most likely the input FET's. There are a couple of ways to check the FET's, but probably the fastest way is to remove the second stage. In the case of the Input Amplifier, remove A55Q1A/B.

Connect an -hp- Model 419A across the drains of A71Q1A/B. That is, connect the 419A where the bases of A55Q1A/B were connected. Using A55R14 should be made to read zero and hold zero plus or minus a few hundred microvolts. If this is not the case, the FET's are bad. This will mean that A71, the peltier chamber will have to be replaced. The cooler drive circuit should be checked to see that it is operating properly. See paragraph M.

The Polarity, Ratio-Percent, and Integrator Amplifiers should be checked out using the same procedure as was used with the Input Amplifier. Of course, only the Input Amplifier uses an Auto-Zero circuit. Therefore, start troubleshooting these amplifiers by opening their feedback loops. In the case of the Polarity Amplifier by shorting the junction of A100R4 and A69R8 to the inguard ground. For the Ratio-Percent Amplifier short the junction of A56R20 and A56R37 to inguard ground. For the Integrator, short A57Q5A gate to inguard ground, and tape off A57 pin 5. Be sure to leave the 3450A on MAN/EXT.

If these amplifiers are good, the zero adjust potentiometer will swing the amplifier from positive to negative saturation. Refer to the discussion of the Input Amplifier for the remainder of troubleshooting these amplifiers.

Check for Zero Detect/Polarity Detect Signal

If all the amplifiers check out okay, supply the 3450A with a negative 10 volts DC. Connect one channel of an oscilloscope to A7TP1, the sample period flip-flop. Connect the other channel to the yellow lead on the upper right side of the pulse transformer. This is the base of A66Q1. The pulse transformers are located just behind and to the right of the Nixie tubes. Trigger the scope at A6TP6. The waveform shown in Figure 5 will be observed only if the sample period rep-rate can be slowed down. This would be done with the front panel sample rate potentiometer.

The waveforms shown in Figure 6 will be observed if the sample period rep-rate is not adjustable. The top wave is the sample period and the lower wave is the polarity-detect/zero-detect signal. The negative step is the negative polarity-detect and the positive step is the zero-detect. This waveform will only be seen with a negative input. This is because the polarity-detect signal (negative step) only occurs for a negative input. For a positive input a 2 μsec pulse will occur at the same time as the positive step. Since this zero-detect is fast and occurs at a slow rep-rate it would be more difficult to see. If these waveforms are present, then the problem is either the pulse transformer or perhaps the zero-detect flip-flop, A6IC20. If the signal is not present, check the circuit between the integrator output and the pulse transformer. This consists mostly of three IC analog amplifiers.

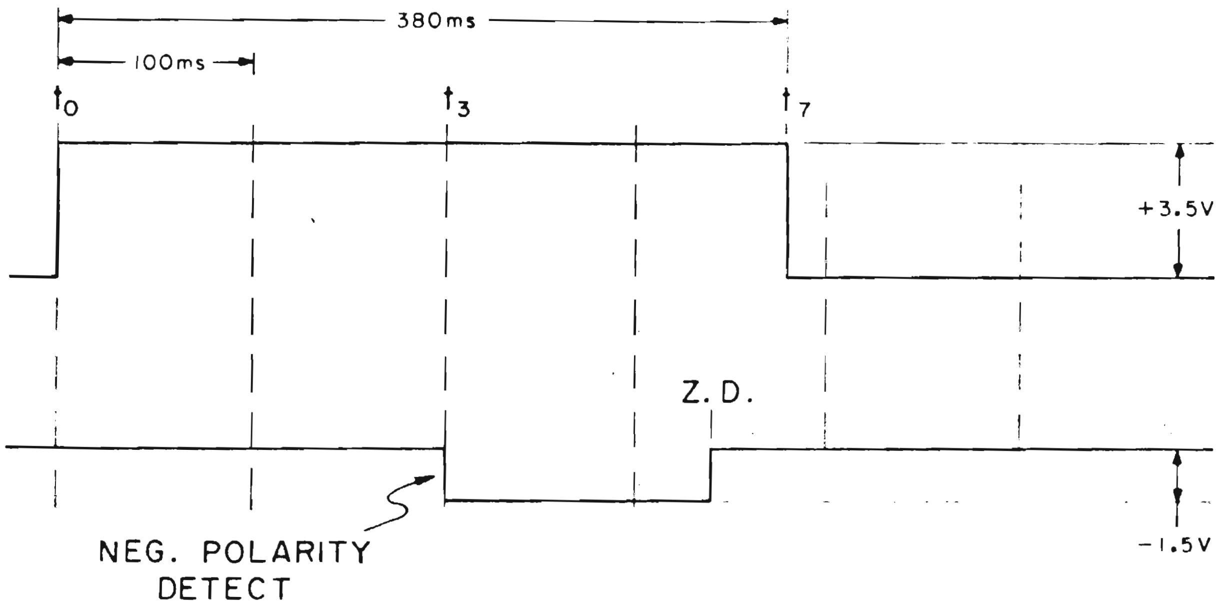


Figure 5. Polarity/Zero Detect signals with rate control.

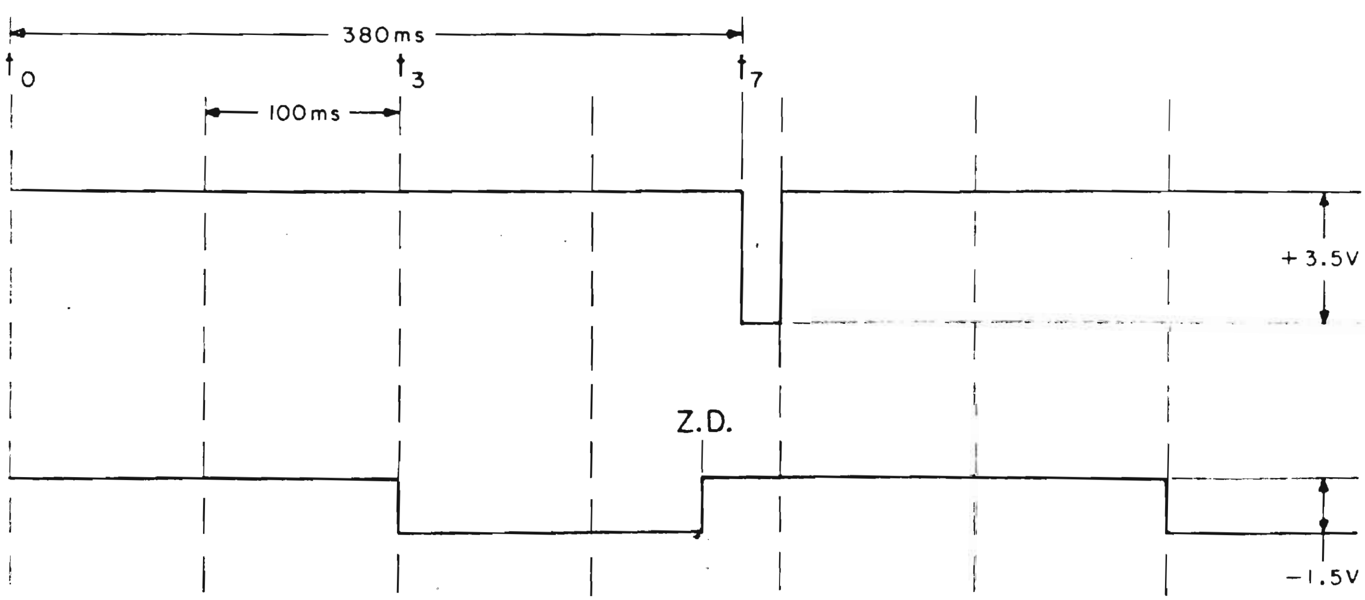


Figure 6. Polarity/Zero Detect signals with no rate control.

To check the zero-detect flip-flop, use a logic probe or oscilloscope and observe the pulses on the output A6IC20 pin 2. There should be a pulse here for each sample. If not, check the input to this IC and the output from the pulse transformer. Another check for the pulse transformer output is to check the polarity flip-flop A5IC11 pin 14 should alternate with a negative input and remain low always for a positive output.

If the amplifiers all check out, the only other signals to be checked are the reed relay drives, electronic switch and the polarity strobe.

Reed Relays

The reed relays that are required to operate on DC, non-ratio are given in table 2. The time intervals that are given are the time periods that the relays are closed. There are other relays that are closed or open during the entire sample period, but these relays are not included in this table.

RELAY	TIME CLOSED
K4 or K5	${}_0T_3$
K7	${}_3T_0$
K8	${}_3T_7$
K9	${}_3T_0$
K10, K11, or K12	${}_0T_3$
K14, K15	${}_3T_{ZD}$
K17 (WITH + POLARITY)	${}_7T_3$
K29	${}_{ZD}T_{0'}$

TABLE 2.

This only checks the coil and, of course, the reed may not actually be closing. A continuity check will determine the state of the relay. The closure of these relays are timed with the charging curve. The best way to see that the relay drives are occurring at the proper time is to use one trace of an oscilloscope on the Integrator output and the other trace on the reed relay. Refer to page 7-5 in the Operating and Service Manual. The various timing points on the Integrator waveform are given. Also, the chart below the Integrator Waveform gives the timing of all the reed relays.

Electronic Switch

The Electronic Switch signal is coupled through the pulse transformer to the A60 inguard logic board. The signal originates on the A6 board and at the input to the

A60 board it is 0.5 μsec pulse. This pulse is used to toggle the G binaries. G_1 and G_1 are used to control driver transistors A60Q1/Q2. The output from A60Q1/Q2 turns on and off the FET switch on A57 circuit board. The best way to check out this circuit is to start at the output of A60Q1/Q2 and keep checking back until the fault is found. A logic probe would work very nicely. Note, the 0.5 μsec pulse is very difficult to see on an oscilloscope. Turning up the intensity will help.

Polarity Strobe

The Polarity Strobe signal is generated in almost exactly the same manner that the Electronic Switch signal is generated. The only difference is that the Polarity Strobe uses the G_2 signal. Again, troubleshooting could start at the output of the A60 circuit board, A60Q31, and proceed back to the fault.

F. Ranging. The ranging of your instrument can be considered in two sections or modes. First, and least complicated, is the non-ratio mode. The other, more complicated mode, is ratio operation. Ratio is more complicated because, the range changes three times in one ratio sample period; the first range change is to measure Y, the second range change is to measure X, and the final change back to Y range.

To begin troubleshooting the ranging circuits of the 3450A, set the functions to HOLD, DC, and place a short across the input. The first check will be of the Primary Range Binaries; P_1, P_2, and P_4 on A8IC2, A8IC3, and A8IC5. By stepping through the ranges, these points should change state according to the Primary Range table given on the A8 schematic page 7-19 of the Operating and Service Manual.

If the Primary Range Binaries do not count, check the inputs and outputs of A8IC1 as follows:

1. In AUTO, Pin 4 is high.
2. Pin 5 is oscillating at the sample rate.
3. Pin 3 is low in AUTO and will oscillate if you go to HOLD and step through the range. If Pin 3 does not oscillate, the Up/Down Range Enable is not functioning. This signal is generated on A9 (Figure 7-11). The Up Range Enable and Down Range Enable are OR'd together to give the Up/Down Range Enable signal. To check the Up-Range flip-flop and the Down Range flip-flop, place a short across the input. In DC, non-ratio, the 3450A will be on the 100 mV range and Pin 2 of A9IC20 will be high. Now go to HOLD and Step up to the 1 kV range. Place the instrument in HOLD and step through the ranges, monitoring A9IC10 Pin 14. When you reach the 100 mV range, the instrument will overload and A9IC10 pin 14 will go from a constant high state to an oscillating condition.
4. Pin 11 is high.
5. Pin 12 is high except for the recycle pulse received when going from the mV range to the kV range.

6. Pin 13 will go high when Step is depressed. If this does not happen, check A8IC10 Pin 9 to verify that a pulse is received from A4 when STEP is depressed. If no pulse is received, check A4IC13 and A4IC14 for proper operation.

The next check to make is Primary Range Decoding. A8IC13 and A8IC14 outputs produce the proper P Rng 10^X signals. These can be compared with the Primary Range table as the ranges are stepped through. If both the Primary Range Binaries and the Primary Range Decoding is functioning, but the binaries don't recycle properly, check A8IC1 Pin 12 for the recycle pulse between 100 mV range and 10 kV range. If this is not present, check the inputs and outputs of the Primary Range Recycle circuit.

If the Primary Range Binaries and the Primary Range Decoding checks out correctly, we will focus our attention on the Input Range Encoding. We can check the outputs of A8IC22 and A8IC8 against the Input Range table on Page 7-19 to insure correct E_1, E_2, and E_4 signals. If these signals are not present as you step through the ranges, only part of the Input Range Encoding will have to be checked. Pin 14 of A8IC20 is the E_1 output in non-ratio. Pin 2 of A8IC8 is the E_2 output in non-ratio and Pin 14 of A8IC6 is the E_4 output in non-ratio. All of the other outputs of the Input Range Encoding are used only in ratio and will be discussed later.

If E_1, E_2, and E_4 are present, check the Input Range Decoding against the Input Range table to see if E Range 10^X is being decoded as the ranges are stepped. If so, the next step is to check the Channel Relay Drive A2 to insure that the proper relays are being closed when the range signals are present.

The non-ratio ranging checks have now been completed. To finishing the ranging troubleshooting, the Ratio Multiplier Range Binaries, the Multiplier Range Decoding and the remainder of the Input Range Encoding must be looked at.

To begin set the functions to DC, Hold, and Ratio. Put 1 volt across the X and Y terminals. While stepping through the ranges, check out the output M_1 and M_2 from A9IC16 and A9IC15 against the Ratio Multiplier Range table on page 7-21. If the Ratio Range Binaries are not counting properly, check the inputs to A9IC17 as follows:

1. In AUTO

   Pin 9 is low
   Pin 10 is switching
   Pin 7 is high

2. In HOLD

   Pin 9 is oscillating
   Pin 10 is oscillating
   Pin 7 is low.
   Pin 3 is high
   Pin 5 pulses for each step
   Pin 4 pulses once when the Ratio Multiplier Range recycles from the X1000 range to X^1 range.

If the Binaries are counting properly, the next check will be of the Multiplier Range Decoding. By stepping through the ranges and observing the outputs of A9IC2, A9IC1, and A9IC3, the M Range X signals can be compared with the Ratio Multiplier Range table. If the Binaries are counting and the Range Decoder is functioning but the Binaries won't recycle properly, check Pin 4 of A9IC17 for a recycle pulse between the X1000 range and X1 range. If this signal is not present, troubleshoot the Multiplier Range Recycle circuit.

If both the Ratio Multiplier Binaries and the Multiplier Range Decoding are correct, our attention returns to the Input Range Encoding on A8. This can be checked by stepping through the ranges, noting the output of the Range Encoding for each range (E_1, E_2, and E_3). Sample period has to be stopped in the $_7T_8$ interval by grounding the top of A6R3. This ground must be removed each time range is to be stepped.

G. Function. The Front Panel Assembly is shown on Figure 7-16 of the Operating and Service manual. A30 is comprised of A11 and A12. The signals used to set up the function of your instrument are generated by this assembly, transported by flex cable to the A4 board, and used to generate the proper logic to control the instrument's operation.

Begin by pushing each pushbutton on the front panel and simultaneously observing the output of the appropriate flip-flop on A12. If the flip-flops are functioning correctly, but the front panel light doesn't indicate the function, check the transistor and light bulb on A11 that corresponds to the function. Also, the problem may be caused by the pushbutton spring not being in its correct position. Refer to service note P-4040-0427 for a detailed description about the spring placement.

If the flip-flops are operating correctly, check the inputs to A4 (Figure 7-6 Pages 7-11). The inputs from the A12 board should correspond to the functions selected. If the inputs do not correspond, and the outputs of A12 are correct, the problem is associated with the flex cable.

After checking the inputs, the outputs of A4 become our next concern. Step through the different functions once again, observing the appropriate output for each function. If the outputs of A4 are incorrect, check the outputs of the appropriate flip-flops on A4 for the correct output voltages. Note that ratio voltage level should be about 3 volts instead of 4.4 volts. Also Auto will be about 2.95 volts instead of 4.4 volts.

If while checking out these voltage levels, you find that one or two of the levels are only 1-2 volts and should be 4.4 volts, a loading problem may exist. This can be caused by a shorted gate on some other board. To locate the cause of the problem, tape off the output pin that is low. Check to see if the flip-flop output is correct. If it is correct, refer to Table 3. Tape off the appropriate input to other boards until the signal is restored to its proper value. When this occurs, you have located the board that is causing the loading. Now refer to the schematic to determine which gates could be causing the problem.

Output Function	A4 Pin Number	AX Pin Number
DC	J-A	A2-K-A, A8-3-B, A10-2, A13-2
$\overline{\text{DC}}$	H-A	A2-H-B
AC	L-A	A7-D-B, A2-B-B, A7D-B, A82-B, A9B-B, A10-4, A24-4-A, A25-11-A
$\overline{\text{AC}}$	K-A	A7-F-B, A2-D-A, A7F-B, A92-B
Ohms	N-A	A2-D-B, A8-5-B, A9-7-A, A10-1, A24-C-A, A25-X-A
$\overline{\text{Ohms}}$	M-A	A9-8-A
Ratio	10-B	A2-C-A, A7-11-A, A9-6-A, A10-3, A25-N-A
$\overline{\text{Ratio}}$	11-B	A3-F-B, A8-C-A, A9-3-A
L. T.	J-B	A24-20-A, A25-5-A
$\overline{\text{L. T.}}$	M-B	
Auto	14-A	A9-7-B
Hold	13-A	A9-D-B
$\overline{\text{Step Initiate}}$	B-A	A8-3-A
1/60 Sec Gate En	3-B	A2-S-B, A5-H-B
$\overline{\text{1/60 Sec Gate En}}$	2-B	A5-I-A
$\overline{\text{10 M}\Omega\text{ Input}}$	N-B	A2-10-A
Integ Delay	R-B	A2-M-A
$\overline{\text{Integ Delay}}$	S-B	A5-D-B, A7-H-B
Local	R-A	A10-14, A10-24, A10-34, A10-44 A10-54
Rem	P-A	A3-H-A
Over program	A-A	A10-11
$\overline{\text{Samp}}$	14-B	A3-B-B, A25-21-A

TABLE 3.

H. Polarity. If the polarity indication is wrong, the problem is most likely A5IC11. This is the Polarity flip-flop and this flip-flop will switch only for a negative polarity. Other possible problems are A5IC9, A6IC4, A17Q2, or the pulse transformer.

I. Ratio Problems. There are three differences between ratio and non-ratio. 1) Ratio-Percent Amplifier gain, 2) Timing and 3) Ranging. Since this guide contains information for Timing and Ranging troubleshooting, the only information needed here is the Ratio-Percent Amplifier gain. The Δ-20%-Y pulses originate on A7 circuit board and are transmitted through the pulse transformer to the A60 circuit board. Check the relay drive outputs using the chart given on page 7-39 of the Operating and Service Manual. Note that the check marks on this chart indicate when the relays are open.

Use the table given on page 7-45 of the Operating and Service Manual to establish the state of the relay drives. Start with the outputs on A60 and work back into the logic circuit until the fault is located.

J. AC. See the troubleshooting section of the 11078A Operating and Service Manual.

K. Ohms.

I. FRONT PANEL

A. Determine that the problem is really in the ohms section. Since the DC section is used to measure the voltage developed across the "unknown" resistor, the DC section must be functioning properly. Each OHMS range corresponds to a DC voltage input range. The correspondence is shown in the table below. Using this table, apply the indicated DC voltage for each OHMS range that malfunctions.

Ohms	DC
10 M	10 V
1 M	10 V
100 k	1 V
10 k	10 V
1 k	1 V
100 Ω	100 mV

If the instrument works properly in DC, but not in Ohms, the problem is probably in the ohms section.

There are six general areas to cause problems in the ohms section.

I. Ohms Amplifier
II. Feedback Loop
III. Ohms Reference Voltage
IV. Power Supply
V. Logic and/or Reed Relays
VI. Overload Circuit

I. Ohms Amplifier is a differential Amplifier and is made up of transistors A72Q1, 2, 3, 4, 5, 6, 7.

II. Feedback Loop consists of the resistor "stick" A58R1 - R9 and the associated reed contacts.

III. Ohms Reference Voltage is the 9.09 volts developed across A59CR5.

IV. Ohms Power Supply ±(30 V ±2 V) is separate from the other inguard supplies and has its own reference.

V. The Ohms Logic is used to close the proper reed relay in accordance with function, range and timing.

VI. The Overload Circuit consists of A72CR2, CR3, CR4, Q8, R16 and R17. This limits the externally applied current to a maximum of 4 mA up to 200 V.

The front panel indications can help eliminate some of the basic parts of the ohms section.

A couple of examples may help:

1. The instrument works only on some ranges. The problem is most likely in the Ohms Logic or Feedback stick.
2. The instrument fails only in ohms ratio. The only thing different about ratio and non-ratio is the logic and two reed relays (K30A and B).
3. The instrument malfunctions in all ohms ranges. Any of the basic parts of the ohms section could be the cause. The following sections will discuss troubleshooting for each circuit in the Ohms converter.

OHMS OVERLOAD

The ohms overload circuit consists of two sections. (1) The input protection (current limit) and (2) The excessive voltage circuit.

(1) The current limit consists of A72Q8 and CR2. Q8 limits the current from a positive source (with respect to 3450A front terminals) to 4 mA up to 200 V. CR2 limits the current from a negative source to its leakage current up to 200 V. A72R16 limits the gate current of the FET and R18 the transient overload current.

(2) Voltage is limited to - 17 and +5 by diodes A72CR3 and CR4.

TROUBLESHOOTING OHMS OVERLOAD CIRCUIT

A. Input protection circuit (A72Q8).

A failure of A72Q8 will show up most on the 10 kΩ range. The voltage applied to the unknown resistor will not track as larger values of resistors are placed across input terminals. The current applied to the unknown resistor will not remain constant with increasingly larger values of unknown resistance. The current should be 900 μA for the 10 kΩ range. The front panel indication would be, for the 10 kΩ range, an increasing error as full scale (10 kΩ) is approached.

B. Excessive voltage circuit.

This is protected by CR3 and CR4. The fastest way to check this is to simply lift the yellow and blue leads from CR3 and CR4. If instrument is working correctly with these leads lifted, replace the leads one at a time. This will determine if one of the diodes is faulty.

OHMS AMPLIFIER

The amplifier consists of 4 stages of differential gain followed by an emitter follower. The input stage is a differential pair of FET's. The FET leakage current is approximately 25 pA, and the amplifier open loop gain is 100,000.

TROUBLESHOOTING OHM AMPLIFIER

The first step is to put the amplifier in a unit gain condition. This is done by connecting the output (black wire on K35) to the input (gate of Q1A). Unsolder the red lead from the 9 V reference to the gate of Q1A. The output (emitter of A72Q7) should be less than 30 mV. If this is not the case, each stage of the differential amplifier must be checked out. Before doing this, a little word concerning Q2. This transistor is a 1854-0221; they have given some problems. This is what you might call "educated shotgunning."

The best procedure to check out the differential amplifier is to measure the differential voltage levels from side to side of each stage. The differential voltage should be less than a few mV. These measurements could be made with a 419A, and an example of this measurement would be from the base of A72Q3 to the base of A72Q4. Also, the 3450A should be in MAN/EXT for this test.

Figure 7 on the following page has some "nominal" voltage levels. All of these were measured relative to ohms amplifier ground, not inguard ground, and a 419A was used. The levels may vary from instrument to instrument. The real important levels are the differential voltage from each side of each side.

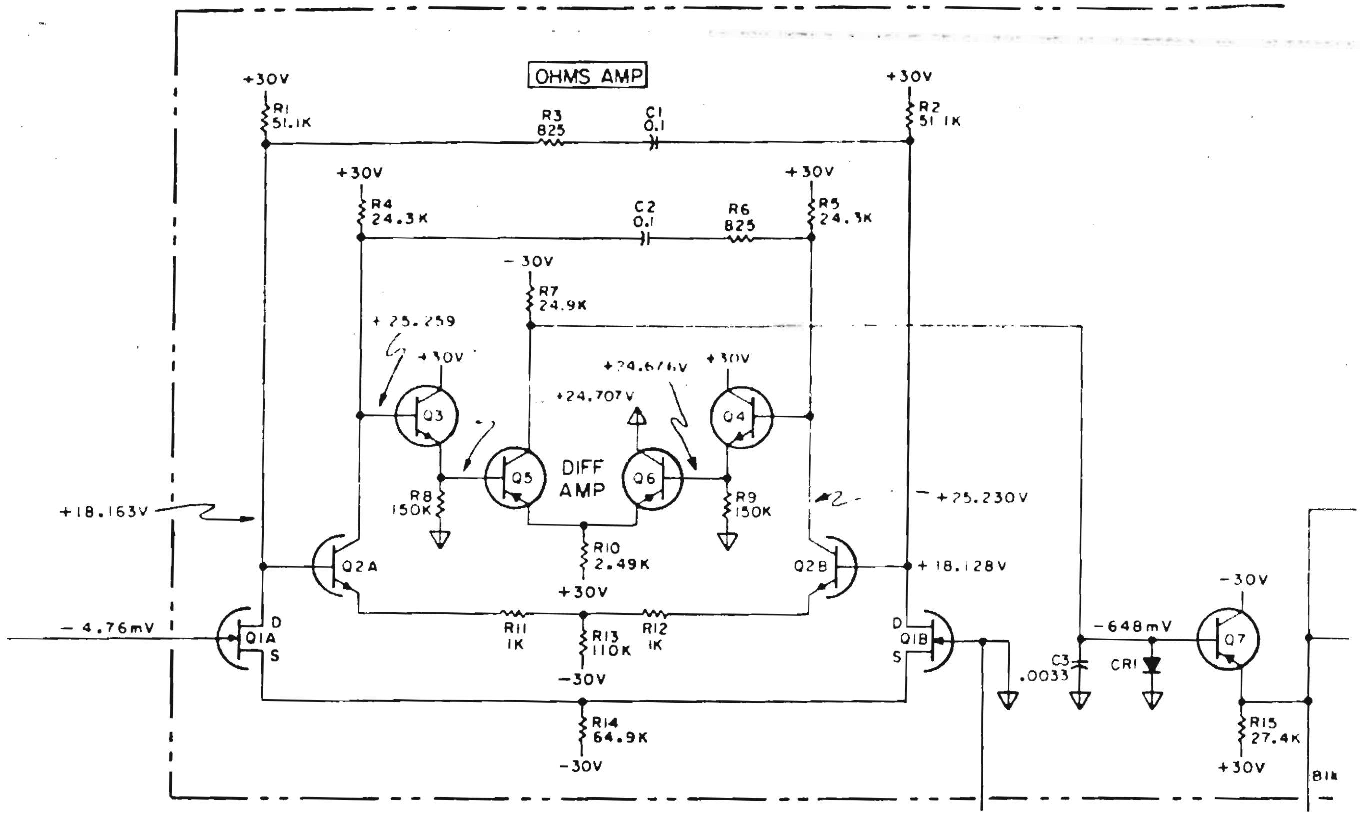


Figure 7.

POWER SUPPLY

This is a relaxation oscillator. R2 and T1 determine the frequency of oscillation which should be 20 kHz ±3 kHz. The frequency is affected by the load and will increase with load. The rectified and filtered output of the secondary is ±30 V ±2 V).

TROUBLESHOOTING POWER SUPPLY

If the oscillator does not operate, check out A59Q2 and Q3. If the oscillator still does not oscillate, transformer T2 may be the problem. Transformer T2 may be checked out by replacing the primary windings with two 150 Ω 1/2 watt resistors. This is done by disconnecting the primary windings and soldering the resistors into the circuit. If the oscillator will now operate at 20 kHz ±3 kHz then replace T2.

LOGIC AND REED RELAYS

The logic circuits perform two functions. 1) Closes the appropriate reed relays for ranging, 2) Closes the reed relays to connect ohms section to Y_{HI} and Y_{LO} (also X_{HI} and X_{LO} on ratio).

Table 4, on the following page indicates the logic states for each IC referenced to the input range. The other IC's are controlled by timing signals.

Table 4.

INPUT RANGE	IC1		IC2		IC3		IC4	
	HI	LO	HI	LO	HI	LO	HI	LO
10MΩ	5,6,10,11		11,12,13	9,10,14	5,6,14	10,11,12,13	2,3,5,6, 10,11,12,13	4,14
1MΩ	5,6,10,11		11,14	9,10,12,13	5,6,14	10,11,12,13	3,4,5,6, 10,11,12,13	2,14
100KΩ	5,6,10,11		11,14	9,10,12,13	5,6,14	10,11,12,13	3,4,5,6, 10,11,12,13	2,14
10KΩ	5,6,10,11		11,12,13	9,10,14	5,6,10, 10,12,13	14	2,5,6, 10,11,12,14	3,4,13
1KΩ	5,6,10,11		11,12,13	9,10,14	5,6,10, 10,12,13	14	2,5,6, 10,11,12,14	3,4,13
100Ω	5,6,10,11		11,14	9,10,12,13	5,6,10, 10,12,13	14	2,5,6, 10,11,12,14	3,4,13

FEEDBACK LOOP

The feedback loop provides a known and accurate reference resistance. There is not too much that could happen to this circuit. The problems that could occur are: (1) wiring butch, (2) bad resistor, or (3) a bad relay.

OHMS REFERENCE (9.09 V ±50 mV)

To measure this voltage, connect the negative lead of an -hp- Model 419A to K30B or K31B and connect the positive lead of the 419A to the violet lead on K35A. The negative lead of the 419A may then be moved to the green lead on K34. This will check that these relays (K30, K31) are working. If no voltage is found, measure the voltage across A59C1. The AC voltage coming to the board should be 10 V RMS ±2 V.

L. MASTER TIMING. The following tests examine the master timing circuits. Also, a block diagram of this Master Timing Loop is located on Page 29. The 3450A can generate a sample period with only the outguard power supply (A14), A5, A6, and A7 boards in the instrument. Remove A2, A3, A4, A8, A9 - the outguard assembly boards.

With these boards removed, the overload light and all of the function lights will be displayed. The rate light will be flashing at an odd frequency. This is caused by both the not 1/60 sec Gate enable and 1/60 sec Gate enable signal inputs to the A5 board being in the true state. This enables both the 1 MHz and 6 MHz signals to be passed through the count gate, A5IC8. You should have rate control. If you have no control over the sample rate, check out the rate delay circuit on A7.

If you will look at the input to A5, A6, and A7, and the outputs of A4, you will notice that the sample period is controlled by A4. Therefore, by grounding the proper output of A4, we will duplicate the switching done by A4. This switching can be noted by watching the rate light on the front panel or by observing A7TP1, the sample period waveform.

The first step is to ground A4 2-B and A4 10-B. The instrument is in DC, non-ratio, fast gate (1/60 gate enable). By opening A4 2-B and ground A4 3-B, the instrument will go to DC, non-ratio, slow gate (1/10 gate enable). The light will flash at 1/6 the rate as fast gate. If either of these symptoms are not noted, check A5IC8. Make sure that both 1 MHz and 6 MHz can be obtained at the output.

Now, ground A4 K-A. This gives you AC non-ratio slow gate. If the rate light does not decrease considerably, check Integration Delay circuit on A7.

Next, we want to check out the ratio timing. In ratio mode, the sample period is doubled. Start by opening A4 K-A. We are back to DC, non-ratio, slow gate. Now, open A4 10-B. The instrument will be in DC, ratio, slow gate (the light will flash at 1/2 the rate as before). If ratio timing is not observed, check A7IC12 Pin 11.

This should be high. IC12 Pin 6 should be flipping at the ratio rate. If IC12 Pin 11 is high and Pin 6 is not flipping, check IC8 Pin 7. This should be changing at the ratio rate. If this is not flipping, check out XFER delay, A7IC6.

We have now checked out the sample period in DC ratio, DC non-ratio, AC ratio, AC non-ratio, fast gate and slow gate. If all checks were positive, the master timing is functioning properly.

M. Cooler Drive. Refer to the Sales Amplifier at the end of this guide for a discussion of the Peltier Chamber and the cooler drive circuit.

Although it is not indicated on the Cooler Drive circuit diagram given in the Operating and Service Manual, Page 7-35, there is a test point located between the emitters of A100Q5 and A100Q6. This TP is physically located on the inguard mother board. It is on the top of the mother board between circuit boards A59 and A60.

Connect a 419A from this TP and inguard ground. When the 3450A is first turned on, this voltage should be a negative 4 volts and in about 30 seconds decrease to a negative 1.5 to 2 volts. If this is the case, the drive circuit is working properly.

N. 10 Volt Reference Supply. Since the reference diode, A71QCR1, is located in the Peltier Chamber, the cooler drive circuit must be functioning properly. See Paragraph M.

Refer to the Operating and Service Manual, Page 7-37. There is a TP electrically located between A55R35 and A55R36. Physically this TP is located just below A55R36 on the A55 circuit board. This TP should be at plus 6.8 volts. If this is not the case, make the following checks:

1. Check contact resistance of interconnection, A70 pin 9, 10, and 11 and A55 pins 2, 3, 6, 7, F, and 8.

2. Check transistor A55Q12A/B.

3. Check emitter-base voltage of A71QCR1.

4. The above is a list of the most common failures. Other failures are certainly possible. Check out each transistor and diode using the circuit diagram in the manual.

THE QUICK FIX

100 mV, 1 V and 10 V ranges okay, but 100 V and 1 kV range is noisy.	K5 open.
100 mV, 1 V, 10 V ranges read about one-half input, but 100 V and 1 kV read okay.	K5 stuck closed.
With 9 V input: 1 kV and 10 V range read okay, but 100 mV, 1 V range read 20053 and 100 V shifts decimal.	K9 stuck closed.
1 kV range reads ±13 counts with input open.	K29 open.
NIXIES all blanked.	A13Q13
Nixies function display either doesn't work or displays one function all the time.	A13IC6
Input amplifier has a small drift.	K7 open.
Instrument is very noisy with short on input and will not read voltages.	K1 open.
Inguard +5 volt power supply reads zero or close to zero.	A100Q1, A53CR3
Front panel buttons are not operative; or more than one function on at one time.	Spring contacts (See Service Note P-4040-0427)
Ohm's works on non-ratio but not on ratio.	K31A/B or A59IC1 or IC2
Read + polarity always.	A5IC11
Guard shorted to chassis ground.	Check positioning of all tinnermans.
Reads one polarity correctly, but not the other.	Check the reference supply switching reed relays. K13, K14, K15 or K26.
Sample rate is at some inconsistant frequency.	A5IC8; both 1/60 gate and 1/10 gate enabled.
200 volt power supply not present on A13 board. All NIXIES including polarity and function blank.	Check for poor inter-connection between A10 and A13.

Master Timing Loop

There are two block diagrams of the Master Timing Loop. A simplified diagram is contained in the overall instrument block diagrams on Page 2 of this guide. A more detailed diagram is on Page 29 of this guide. The operation of the timing circuit is explained in the following paragraphs. The "map" given on Page 28 is used to locate the various signal in the timing loop. The alpha points given in the "map" refer to both timing block diagrams.

A. Trigger.

A trigger signal from A7IC1 begins the sample period at t_0. This signal, INT TRIG, is a pulse and switches A7IC5, the sample period flip-flop. It is really the rate-delay f-f, A7IC1, which is a one shot that defines the beginning of the sample period. This one shot is toggled by the presence of 2 signals. Namely, INTERNAL and NOT SAMP.

The above tells how the sample period begins. The sample period is ended by the XFER pulse at Pin 14 of A7IC5. How this signal is generated will be covered in Step 7.

B. Sample Period.

This is simply the sample period itself. That is, the waveform present at the output of the sample period flip-flop, A7TP1. This test point is used in the service guide. The waveform present is a square pulse of either 380 ms (for DC Slow gate) or 65 ms (for DC fast gate).

C. Counter Reset.

The leading edge of the sample period wave is used to reset the crystal oscillator Data Counter. There is quite a bit going on to generate the signal for the counter reset one shot.

First of all there are several different conditions that require the data counters be reset.

The first counter reset is at t_0. This is done by AC coupling the output of A7IC3 to the counter reset one shot, A7IC10. This then generates a $RESET_C$ signal.

At the end of a sample period we may want to reset the data counters, but not have an XFER. The above method of generating a $RESET_C$, the t_0 reset, won't work if XFER does not occur. This is because A7IC5 won't switch without an XFER signal. One time that we would not want a transfer and still want a $RESET_C$ is if we were in Auto and not on the proper range. A7IC9 allows us to $RESET_C$ without an XFER.

Another case where $RESET_C$ is needed without an XFER is in RATIO. If we are on RATIO and are not OVERLOAD MAX, (overload on maximum ranges) then the counters must be reset at T_7 in order to start the X integration (second integration on ratio).

There is only one other condition that generates a $RESET_C$. That is Turn-On.

There are two other times that the data counters need to be reset. At T_3, the end of the charge up period, the counters are reset; and on Ratio the correspond. charge up time – T_{10}. Both of these signals are generated on A6 and decoded on A5. Since these two timing points are critical to the basic accuracy, they originate with the crystal oscillator.

The gate that combines these two methods of resetting the data counters is A10IC5.

Once the data counters have been reset, then they must be provided with pulses to count. This, of course, is done with the 6 MHz crystal oscillator. Before the oscillator counts are made available to the data counter, they are somewhat conditioned.

1) <u>1/10 or 1/60 Gate</u>. If we are using the slow gate, the 6 MHz signal has to be divided by 6. This is done by A5IC5, IC6, and IC7. Either fast or slow gate is selected by use of an "AND" gate, A5IC8.

2) <u>Count Gate</u>. The count gate enables the data pulses to pass to the data counter. There are certain times that we do not want pulses to be counted. They are:

   a. <u>INTEGRATION DELAY:</u> Integration delay is 100 ms on DC and must be programmed to obtain the delay. On AC it is 2.4 sec and is automatically programmed by selecting AC. Integration delay signal is generated on A7. Since these delays are RC types, the 100 ms or 2.4 sec could be changed. Note this circuit has been modified somewhat for H21.

   b. <u>At ZERO DETECT</u> or overload the count gate is disabled. This is simply the end of the measurement. The signal is generated at A6IC20.

   c. One of several delays is the <u>GATE-OPEN DELAY</u>. The purpose of this delay is to account for propagation of the Zero Detect signal. The signal delays the closing of the count gate at the start of each measurement period, (i.e. ${}_0T_3$, ${}_4T_{ZD}$, ${}_7T_{10}$, and ${}_{11}T_{ZD}$)

   d. Another delay is the <u>5 COUNT ADD CIRCUIT</u>. This signal is generated on A5. Be sure to look at the manual change sheet as this circuit was modified considerably.

There is one other count "add" circuit. This one has nothing to do with the count gate. It is located on A10. It is the 10 COUNT SUBTRACT CIRCUIT. A10IC4 subtracts 10 counts since Zero-Detect is not really at zero.

D. N2 - 8'. The data counter provides two timing signals. When the N2 - 8' signal goes false, timing points T_1 and T_3 are generated. When N2 - 8^1 goes false, the data counters are changing from 99999 to 100,000 counts to generate T_1. N2 - 8' goes false again when the data counters change from 199999 to 200,000 to generate T_3.

The N2 - 8' signal originates at A10IC4. These two timing points are for non-ratio. For ratio measurements, there are two corresponding points, t_8 and t_{10}, generated in the same manner.

From A10IC4, the timing signals are AC coupled to an inverter in A6IC13. The output of this inverter is gated with an NAND gate, A6IC13, and enabled by a timing signal. A6IC13 does this for non-ratio and A6IC17 for ratio.

The above described timing signals are the only timing points generated by the 6 MHz crystal oscillator. The other timing points, less critical points, are generated by an astable multivibrator, A5Q10, Q11. The timing points generated this way are t_2, t_4, t_5, t_6, t_7 for non-ratio and t_9, t_{11}, t_{12}, t_{13}, t_{14} for ratio.

E. TIMING ADVANCE.

All of the timing points combine to make up the TIMING ADVANCE signals to the Master Timing Binaries, A6IC5, IC7, IC8, and IC10.

E. Timing Reset.

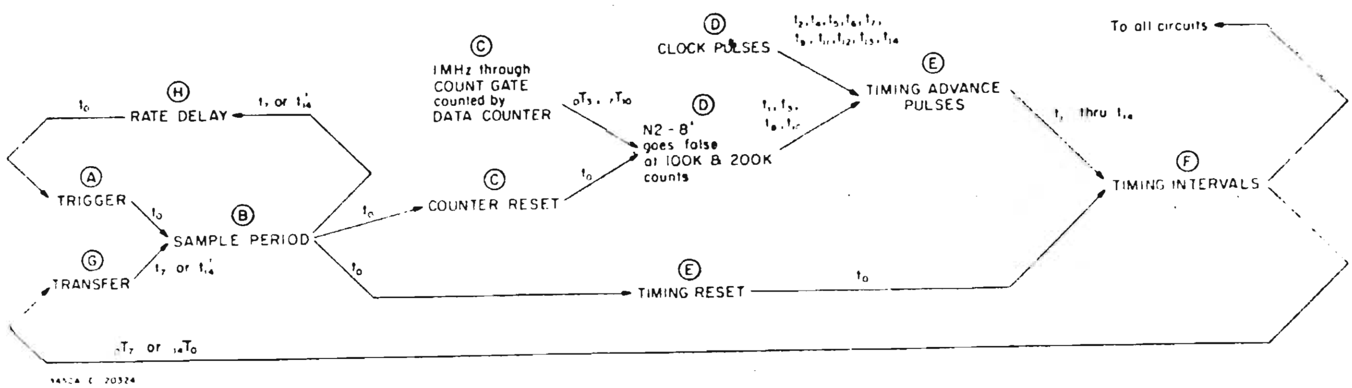
The Timing Binaries are reset in the same manner as the data counters are reset. That is the $RESET_C$ is AND gated with AUTO ranging to reset the timing binaries when the data counters are reset. However, remember that the counters are reset by signals other than $RESET_C$. A7IC10 is where the $RESET_C$ and AUTO are AND gated. A7IC7 and IC11 form the one shot that generates the $RESET_T$ signal. $RESET_T$ is also generated at TURN-ON and at t_o by the SAMPLE signal.

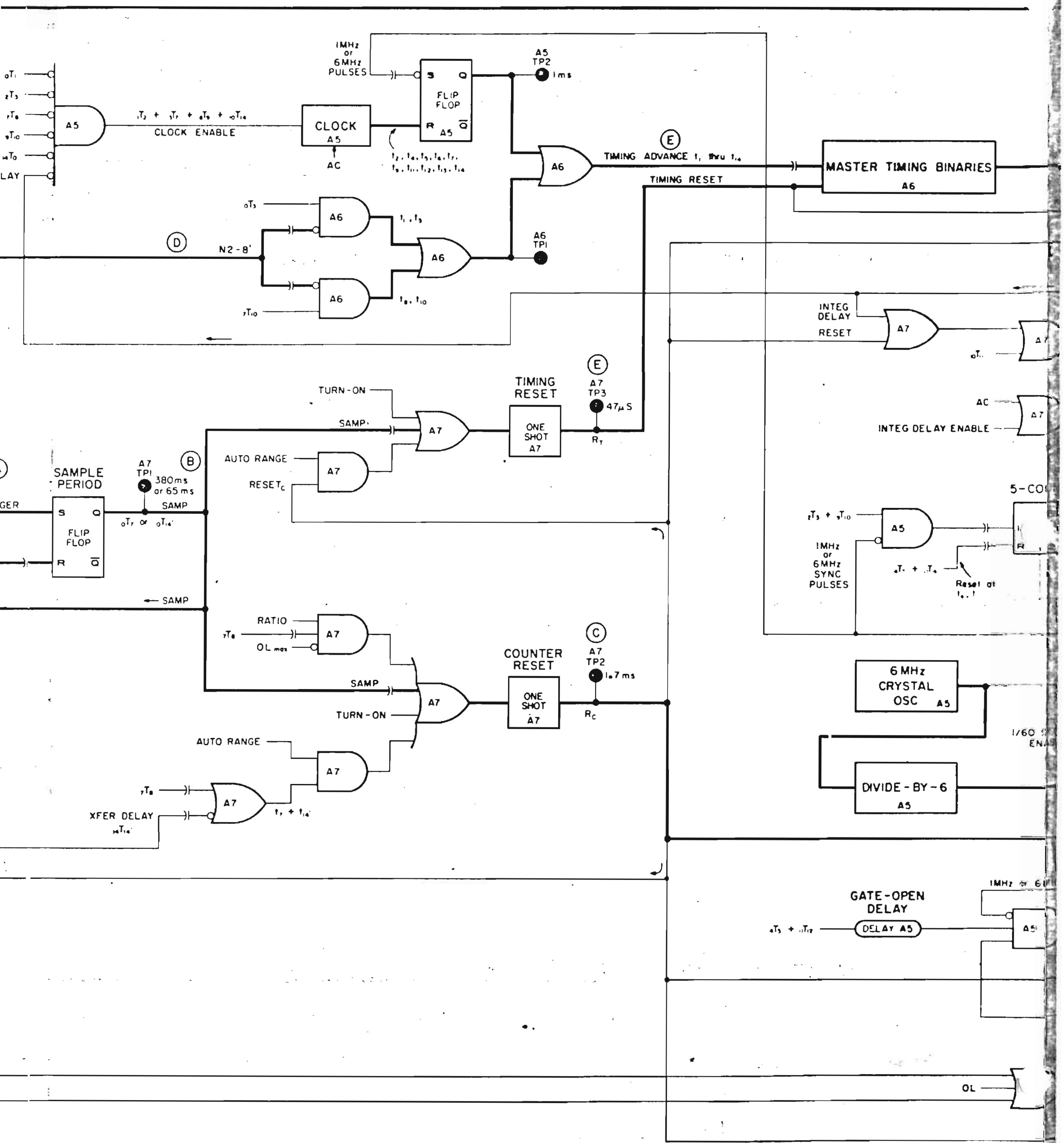
F. Timing Intervals. The Master Timing Binaries are counters and their output must be decoded to arrive at timing intervals. All the timing decoding is done on A6. There are several IC's involved and is generally straight forward. The outputs, timing intervals, are then sent out to the rest of the circuits.

F. Transfer delay A7IC6, is an 80 ms one shot. This IC provides the XFER DELAY signal. XFER DELAY will delay transfer unless we are on ratio or have overload max. Both of the above conditions will be AND gated to provide a signal to the XFER one shot. This AND gate is enabled if we are not AUTO ranging or do not have a Print Holdoff Command.

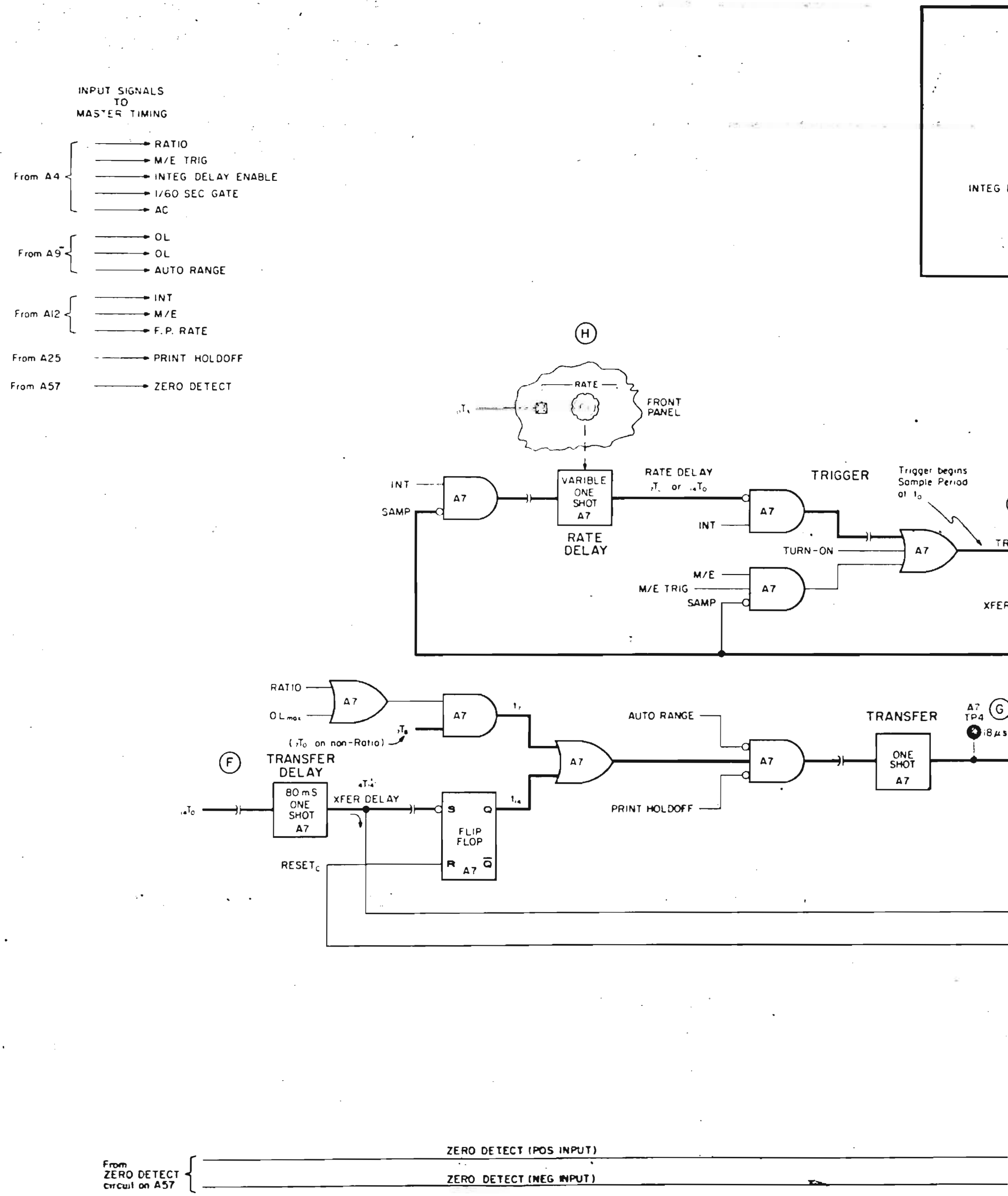
G. Transfer. The XFER signal is generated by A7IC13. The output of this IC is sent to the sample period flip-flop, A7IC5, and ends the sample period. The XFER signal is also sent to A4, A9, A10, A13, and A25.

MASTER TIMING LOOP





1MHz or 6MHz PULSES
FLIP FLOP A5
A5 TP2
1ms
CLOCK A5
AC
CLOCK ENABLE
A5
A6
TIMING ADVANCE t_1 thru t_{14}
TIMING RESET
MASTER TIMING BINARIES A6
N2-8'
A6 TP1
INTEG DELAY
RESET
A7
INTEG DELAY ENABLE
TURN-ON
SAMP
AUTO RANGE
TIMING RESET
ONE SHOT A7
A7 TP3
47μS
SAMPLE PERIOD
FLIP FLOP
A7 TP1
380ms or 65ms
SAMP
5-CO
1MHz or 6MHz SYNC PULSES
RATIO
COUNTER RESET
ONE SHOT A7
A7 TP2
1.7ms
6 MHz CRYSTAL OSC A5
1/60
DIVIDE-BY-6 A5
XFER DELAY
GATE-OPEN DELAY
DELAY A5
OL



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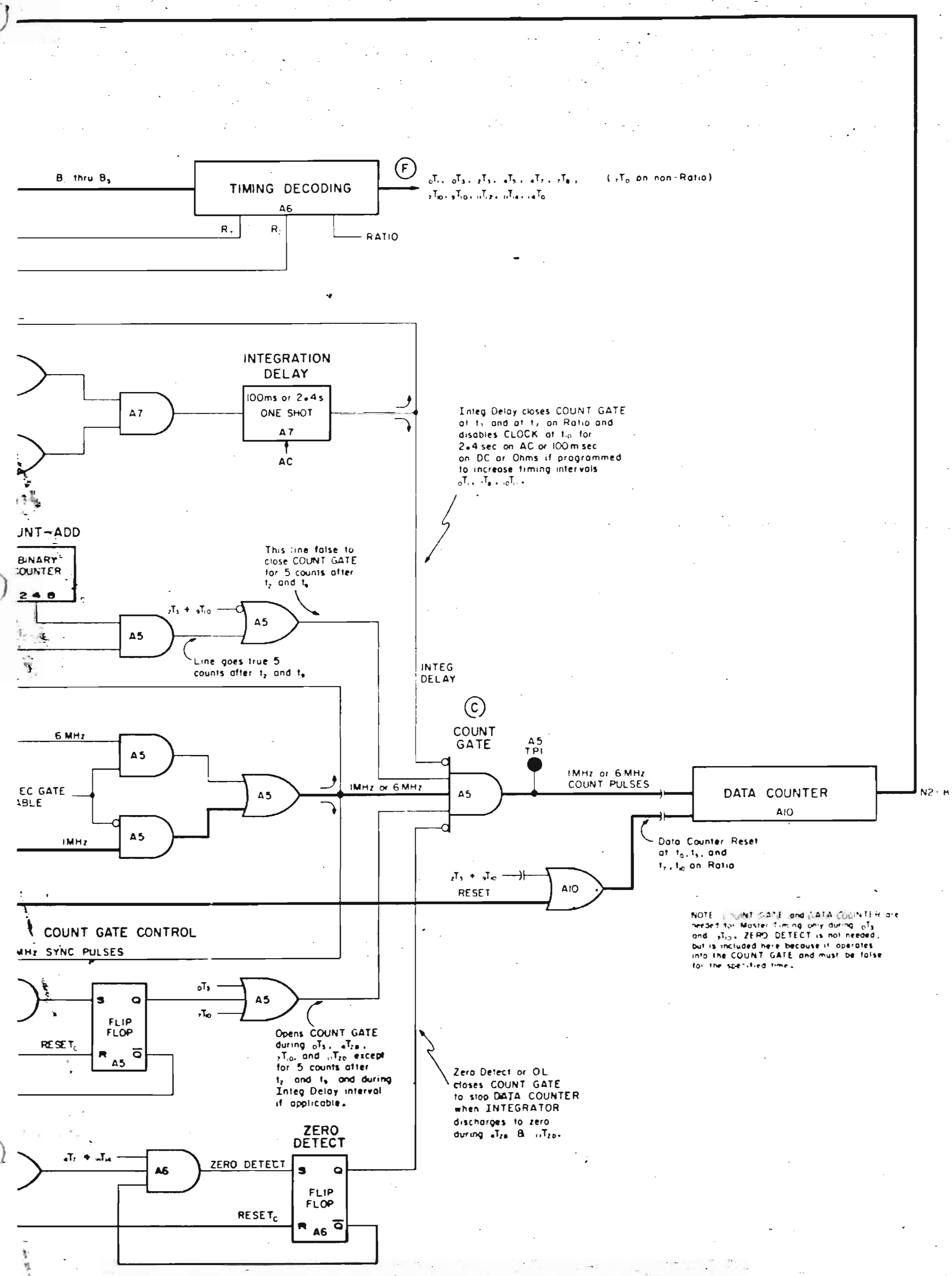
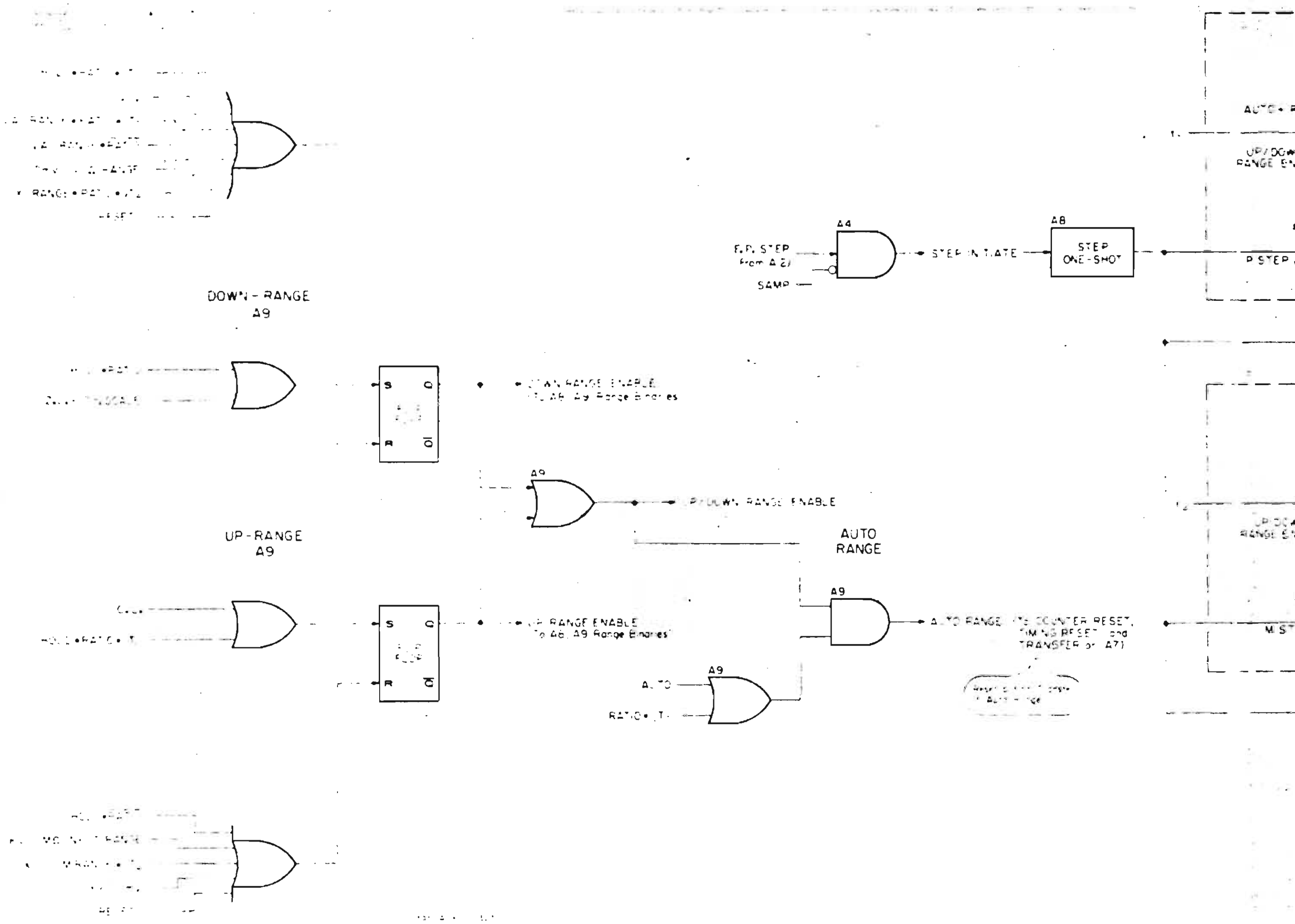
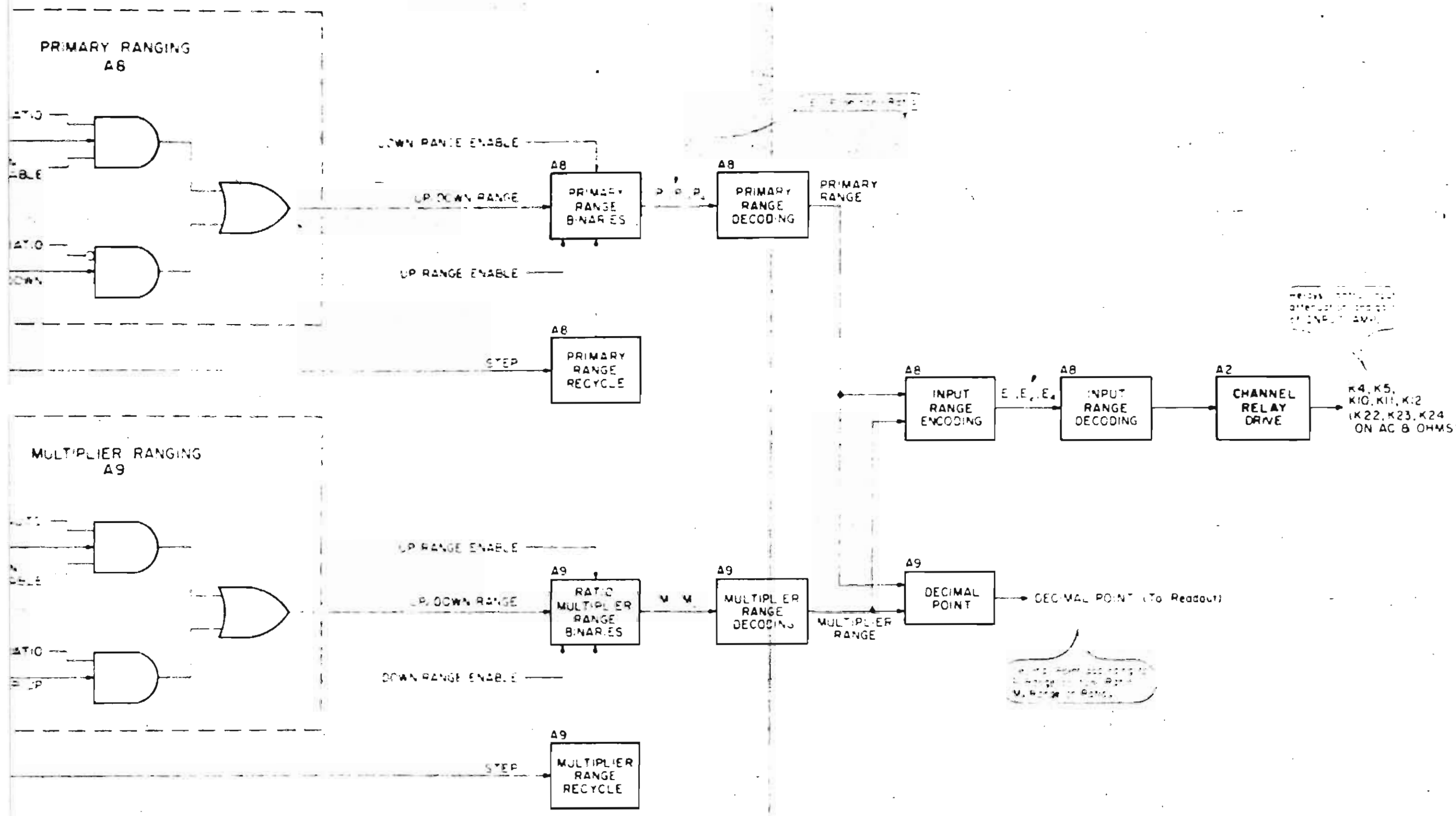


B thru B5
TIMING DECODING
A6
R
R
RATIO
F
(7T0 on non-Ratio)
INTEGRATION DELAY
100ms or 2.4s ONE SHOT
A7
A7
AC
Integ Delay closes COUNT GATE at t1 and at t7 on Ratio and disables CLOCK at t10 for 2.4 sec on AC or 100 m sec on DC or Ohms if programmed to increase timing intervals
BINARY COUNTER
2 4 8
This line false to close COUNT GATE for 5 counts after t2 and t8
A5
A5
Line goes true 5 counts after t2 and t8
INTEG DELAY
C
COUNT GATE
A5 TP1
6 MHz
A5
A5
A5
1MHz
1MHz or 6MHz
A5
1MHz or 6MHz COUNT PULSES
DATA COUNTER
A10
N2-H
Data Counter Reset at t0, t5, and t7, t10 on Ratio
RESET
A10
COUNT GATE CONTROL
MHz SYNC PULSES
NOTE COUNT GATE and DATA COUNTER are needed for Master Timing only during 0T3 and 7T10. ZERO DETECT is not needed, but is included here because it operates into the COUNT GATE and must be false for the specified time.
S Q
FLIP FLOP
RESETC
R A5 Q
A5
Opens COUNT GATE during 0T3, 4T28, 7T10, and 11T20 except for 5 counts after t2 and t8 and during Integ Delay interval if applicable.
Zero Detect or OL closes COUNT GATE to stop DATA COUNTER when INTEGRATOR discharges to zero during 4T28 & 11T20.
ZERO DETECT
A6
ZERO DETECT
S Q
FLIP FLOP
RESETC
R A6 Q



DOWN - RANGE
A9
UP - RANGE
A9
AUTO
RANGE
A4
A8
A9
F.P. STEP
SAMP
STEP
ONE-SHOT
S
Q
R
AUTO

RANGE


PRIMARY RANGING
A6
DOWN RANGE ENABLE
UP/DOWN RANGE
UP RANGE ENABLE
A8
PRIMARY RANGE BINARIES
A8
PRIMARY RANGE DECODING
PRIMARY RANGE
A8
PRIMARY RANGE RECYCLE
STEP
A8
INPUT RANGE ENCODING
A8
INPUT RANGE DECODING
A2
CHANNEL RELAY DRIVE
K4, K5, K10, K11, K12
(K22, K23, K24 ON AC & OHMS)
MULTIPLIER RANGING
A9
UP RANGE ENABLE
UP/DOWN RANGE
DOWN RANGE ENABLE
A9
RATIO MULTIPLIER RANGE BINARIES
A9
MULTIPLIER RANGE DECODING
MULTIPLIER RANGE
A9
DECIMAL POINT
DECIMAL POINT (To Readout)
A9
MULTIPLIER RANGE RECYCLE
STEP

SUPERSEDES
NONE

-hp- Model 3450A Multifunction DVM
(Serial Number 916-00550 and below)

INPUT CIRCUITRY MODIFICATION

The field modification consists of adding a 500Ω resistor (-hp- Part Number 0698-4123) in series with K3 (See Figure 1). Certain instruments, with serial numbers below 916-00551, have this field modification installed at the factory. The field modification should be performed on all other instruments with serial numbers below 916-00551.

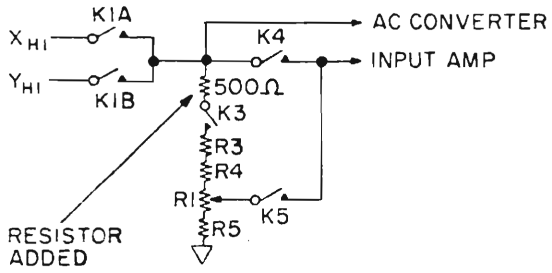


Figure 1.

Instruments above Serial Number 916-00551 will have a slightly different factory modification. The 500Ω resistor will not be added, but the position of K3 and R4 will be interchanged. See Figure 2.

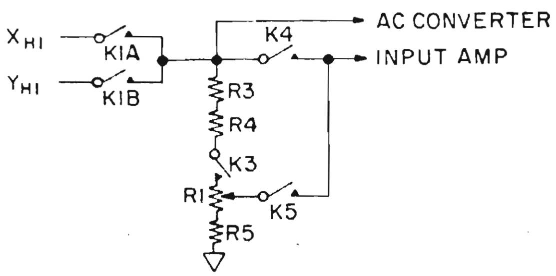


Figure 2.

The purpose of the modification is to increase the charging time of the input circuit. The shunt capacity of the input circuit has caused current spikes on the ground plane of the instrument. These current spikes may damage transistors in the analog portion of the instrument. Also, the spikes may be coupled to the 3450A digital output. The field modification (500Ω resistor) or the factory production change will increase the charging time of this circuit, and thereby reduce the size of the current spikes. The spikes will be most prevalent when sampling large AC or DC voltages.

FIELD MODIFICATION PROCEDURE

CAUTION

USE EXTREME CAUTION WHEN WORKING IN THE REED RELAY CHANNEL. DO NOT ALLOW TEFLON BOARDS TO BECOME CONTAMINATED.

1. Disconnect the K3 pin connector on A68. This is the gray cable going from A68 to K3 relay contacts.
2. Remove the connector on this lead and solder a 500Ω resistor (-hp- Part Number 0698-4123) to end of this lead.
3. Solder a new pin connector on the resistor lead (-hp- Part Number 1200-0162).
4. Slip a short piece of "spaghetti" over the resistor and its lead.
5. Reconnect the new pin connector to the pin on the A68 board.

Perform DC CALIBRATION in accordance with the Operating and Service Manual for the 100 and 1000 volt ranges.

LP/my/wa

July 1969-9

SUPERSEDES
NONE

-hp- Model 3450A Multifunction DVM
(Serial Number 935-01000 and below)

PRINT COMMAND HOLDOFF

A 3450A print command holdoff does not prevent the 3450A from taking a reading when internally triggered; it simply inhibits the generation of a print command after the reading is complete.

This feature optimizes systems speed when the 3450A is used with a printer. When the printer is mechanically ready for new data, the 3450A already has or at least started to digitize the data.

A disadvantage of this scheme is found when trying to use the print holdoff in conjunction with internal triggering to control the 3450A readings. If a print command holdoff is applied to the 3450A immediately after a print command is issued, the 3450A will take another reading and stop. The 3450A will then wait for the print command holdoff to be removed so that it can issue a print command. It is, therefore,possible for the 3450A to take a reading of a new input with the remote commands from the previous reading. This problem can be solved by remotely triggering the 3450A.

Instruments with Serial Number 941-01001 and above may select holdoff at either print command or at internal trigger. Selection is accomplished by positioning a jumper wire on the A7 Sample Period Assembly.

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July 1969-9

Customer Service • 333 Logue Avenue, Mountain View, California 94040. Telephone (415) 968-9200
Europe: 54 Route Des Acacias, Geneva, Switzerland, Cable "HEWPACKSA" Telephone (022) 42.81.50

HEWLETT hp PACKARD

SUPERSEDES
NONE

-hp- Model 3450A Multifunction DVM
(All Serial Numbers)

PHOTOCELL TROUBLESHOOTING FOR AC CONVERTER

The photocell used in the AC Converter may be checked for proper operation by using the following procedure.

IN-CIRCUIT CHECKS

1. Supply a 1 volt rms, 500 Hz signal to the input terminals of the 3450A.
2. On the front panel of the 3450A select AC, INTERNAL, LOCAL, and HOLD. Select the 1 volt range.
3. Adjust A3R24 to provide a 1 volt peak to peak thermocouple signal at A3TP1.
4. Connect an oscilloscope from A3TP1 to reference ground.
5. Switch the input voltage to the 3450A to 10 mV (500 Hz) while monitoring the signal at A3TP1 with the scope. This signal may "ring," but it should not break into complete oscillation. If oscillation occurs, replace the photocell.
6. Switch the input voltage to the 3450A to 100 mV. Again monitor the voltage at A3TP1 for possible oscillation. If oscillation occurs, replace the photocell.
7. Adjust the 3450A input voltage to 1 volt rms (500 Hz).
8. Readjust A3R24 for 720 mV peak to peak at A3TP1.
9. Check A4TP1 for a dc voltage greater than 6.25 volts.

If the photocell fails any of the above checks or if the checks cannot be performed, remove the photocell from the circuit.

A bench check of the photocell may now be performed. This check will require a power supply to drive the lamp, and one or two ohmmeters.

CAUTION

DO NOT EXCEED A LAMP VOLTAGE OF 10 VOLTS OR A CURRENT OF 20 mA. ALSO, DO NOT EXCEED A MAXIMUM R_{LO} VOLTAGE OF 1 VOLT OR R_{HI} VOLTAGE OF 30 VOLTS.

BENCH TEST PROCEDURE

1. Connect a variable dc power supply to the lamp terminals and an ohmmeter to the R_{LO} terminals. If two ohmmeters are available, connect the second ohmmeter to the R_{HI} terminals.

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2. Adjust lamp voltage for a R_{LO} resistance of 200 Ω. Do not exceed a lamp voltage of 10 volts or a current of 20 mA. Measure R_{HI} resistance.

TEST LIMITS: $7.6\ V < V_{LAMP} < 9\ V$
$28\ k\Omega < R_{HI} < 52\ k\Omega$

3. Adjust lamp voltage for a R_{LO} resistance of 2 k . Measure R_{HI} resistance.

TEST LIMITS: $4\ V < V_{LAMP} < 9\ V$

$280\ k\Omega < R_{HI} < 520\ k\Omega$

4. Adjust lamp voltage for a R_{LO} resistance of 20 k . Measure R_{HI} resistance.

TEST LIMITS: $2.5\ V < V_{LAMP} < 3.5\ V$

$2.8\ M\Omega < R_{HI} < 5.2\ M\Omega$

5. Set lamp voltage to zero. Measure R_{LO} and R_{HI} resistance.

TEST LIMITS: $R_{LO} > 500\ k\Omega$
$R_{HI} > 100\ M\Omega$

Replace the photocell if it fails any of the above checks.

SUPERSEDES
NONE

-hp- Model 3450A Multifunction DVM
(All Serial Numbers)

LOW LEVEL LOGIC CONVERSION

The 3450A is convertible to low level logic. (4.4 volts)

Low Level Logic Digital Output Levels

"1": $V_{out} > 4$ V, $R_{out} = 12$ kΩ ±20%
"0": Saturated transistor, $V_{out} < 0.5$ V, $I_{sink} < 12$ mA

Low Level Logic Programming Levels

"1": +2.5 V to +5 V, or open circuit
"0": -0.5 V to +1 V, or grounded circuit

The procedure to accomplish the conversion is:

1. Be sure instrument has a 11099-66501 Rev C (A3) board. If the instrument does not have a Rev C (A3) board, order a new board under warranty. Instruments with Serial Number 913-00401 and above have a 11099-66501 Rev C circuit board installed at the factory. Also, instruments with the following serial numbers have a factory installed 11099-66501 Rev C board:

905-00271	907-00346	911-00383
905-00275	907-00348	911-00386
905-00283	911-00364	911-00387
907-00305	911-00369	911-00388
907-00316	911-00372	911-00390
907-00324	911-00374	911-00391
907-00325	911-00380	911-00398
907-00343		

2. Replace A25R7 with a 1.07 kΩ resistor, (-hp- Part Number 0698-4196).

3. Replace A25R8 with a diode (-hp- Part Number 1910-0016); connect cathode to base of A25Q2.

4. Reposition the jumper wires on circuit boards A3, A6, A24, and A25 for 5 volt logic. If there is any confusion about the correct jumper, measure the voltages at both jumper terminals. Then select the "5 volt" (4.4 volt) terminal.

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SUPERSEDES
NONE

-hp- Model 3450A Multifunction DVM
(Serial Number 916-00800 and below)

REPLACEMENT TRANSISTOR FOR A13Q13

A more reliable transistor has been utilized for the nixie blanking circuit on A13. The new transistor is rated at 1 watt and is used with a heat sink.

The -hp- part numbers for the new components are:

Qty	Description	-hp- Part Number
1	Transistor A13Q13	1854-0234
1	Heat Sink	1205-0205

These component changes should be made whenever an instrument, with Serial Number 916-00800 and below, is in for calibration or repair. 3450A's, with serial numbers above 916-00800, have the new transistor and heat sink installed during production.

It is not necessary to recalibrate the instrument after this repair; however, note these new part numbers in your 3450A Operating and Service Manual.

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SUPERSEDES
NONE

BACKLIGHTED PUSHBUTTON SWITCH BULB REPLACEMENT

A bulb extractor tool, -hp- Part No. 4040-0427, has been developed to facilitate bulb replacement for backlighted pushbutton switches of the type shown below. These pushbuttons are used on the following Hewlett-Packard instruments:

Model 745A AC Calibrator

Model 3370A Integrator

Model 3450A Multi-Function Meter

BULB REPLACEMENT PROCEDURE

1. Place the end of the thumb of one hand over the corner of the pushbutton switch. With the bulb extractor tool in the other hand, place the hooked end of the tool into the front of the slot on the bottom of the pushbutton (Figure 1) and gently push up until the lower end of the pushbutton lens pops out as shown in Figure 2.

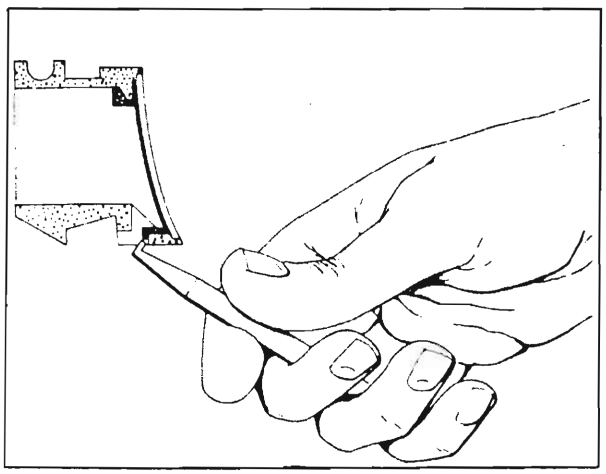

Figure 1

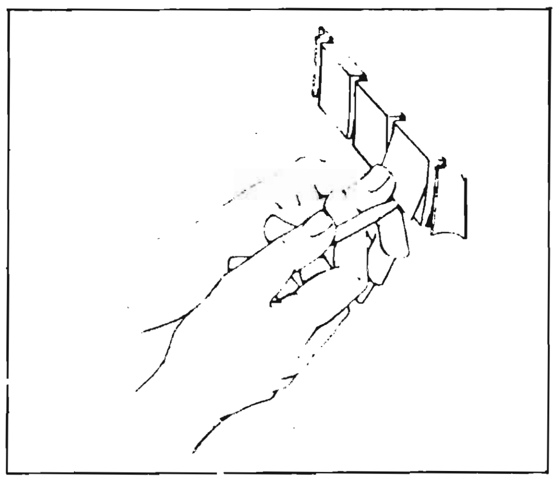

Figure 2

BH/ms

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2. Remove the pushbutton lens. Place the hollow end of the bulb extractor tool over the bulb to be replaced and gently pull back. The bulb should stick in the extractor and come out of its socket as the extractor is pulled back as shown in Figure 3.

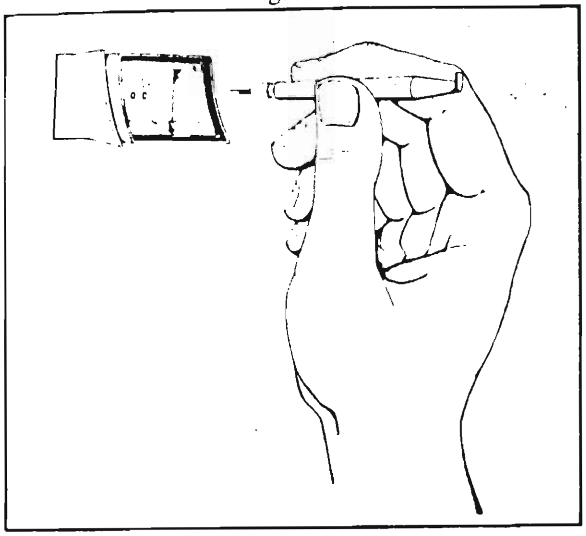

Figure 3

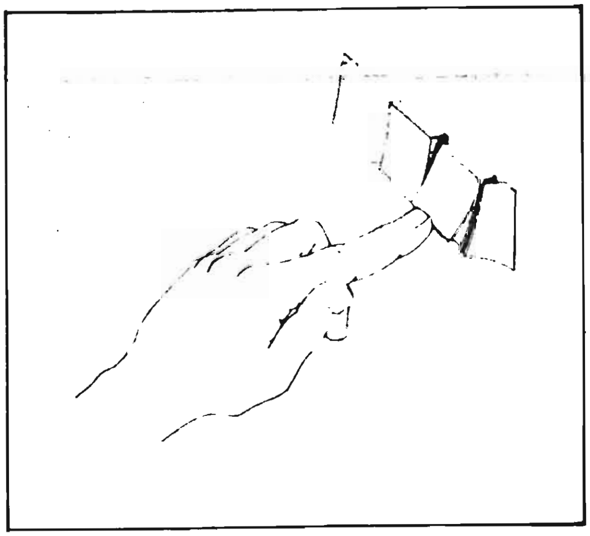

Figure 4

3. Remove the old bulb from the hollow end of the extractor and insert the new bulb into the hollow end. Using the extractor to hold the new bulb, insert the new bulb into the socket. To separate bulb and extractor, gently twist until it easily slips off the bulb.

4. Replace the pushbutton lens by first positioning the tabs at the top of the lens into the top of the pushbutton and pressing the bottom of the lens into place as shown in Figure 4.

CAUTION

ONLY THE PUSHBUTTON LENS SHOULD BE REMOVED FOR BULB REPLACEMENT AND NOT THE PUSHBUTTON ITSELF. IF THE PUSHBUTTON IS INADVERTENTLY PULLED OUT DURING THE REPLACEMENT PROCEDURE, DO THE FOLLOWING:

1. REMOVE THE LENS FROM THE PUSHBUTTON.

2. RE-INSERT THE PUSHBUTTON INTO THE FRONT PANEL.

3. INSURE THAT THE SPRING END IS PROPERLY PLACED IN THE PUSHBUTTON SLOT AS SHOWN IN FIGURE 5.

4. CONTINUE WITH THE BULB REPLACEMENT PROCEDURE.

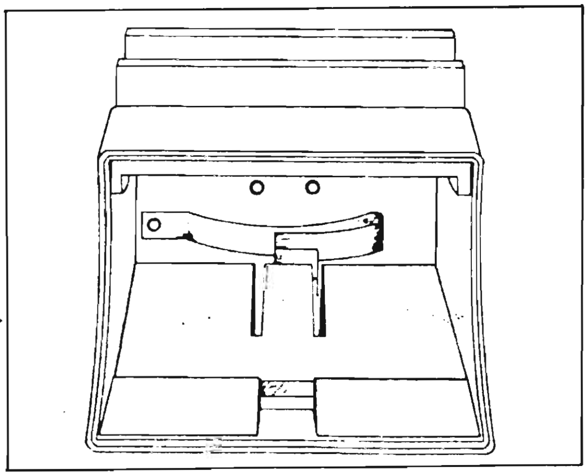

Figure 5

SALES AMPLIFIER

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3450A PELTIER CHAMBER

LOVELAND DIVISION

SEPTEMBER 1968

One of the more impressive advantages of the 3450A is the short time required for the instrument to come to specified operating accuracy after being turned on. The specifications call for 45 s, but as you have probably found out, this is rather conservative. The instrument is usually ready to go in less than 30 s. This is achieved through the use of a Peltier chamber in place of an oven to control the thermal environment of temperature-sensitive components.

This sales amplifier intends to give you a basic knowledge of the theory and operation of the Peltier stability system used in the 3450A by answering these questions -- What is Peltier cooling? How does the Peltier chamber work? What components are located inside the chamber? Why use a Peltier chamber?

WHAT IS PELTIER HEATING/COOLING?

Way back in 1834, a little old French watchmaker by the name of Peltier (he really was a watchmaker) discovered an unusual property of bimetallic junctions. One day he connected a battery across the junction of two dissimilar conductors and noticed that the junction got warm. When he reversed the leads, the junction no longer got warm -- it got cold!

Although he was well-versed in watchmaking, the intricacies of just how the junction heated and cooled depending on the current direction eluded him. If he had had a copy of this sales amplifier handy, he might have found the following explanation helpful.

The heating and cooling effects produced by passing current through a junction of two dissimilar conductors or semiconductors are caused by a change in the energies of the moving electrons.

Figure 1 shows a p-n junction and a representative energy level for each. Let us assume that the

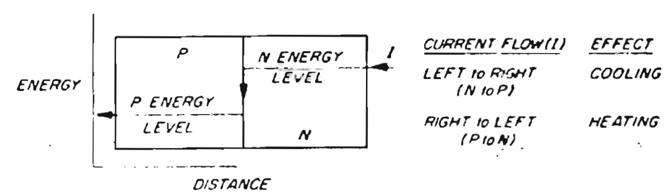


FIGURE 1
ENERGY LEVEL DIAGRAM

electrons in each material are allowed to occupy only the energy levels shown.

Electrons (-I) flowing from left to right must acquire energy at the junction in order to occupy the higher, n-type energy level. This necessary energy is obtained by the absorption of heat. When the direction of electron flow is reversed, the electrons must now give up energy. The required decrease in energy is accomplished by the production of heat.

In summary, electron flow from a p-type to an n-type material causes cooling, while flow from n to p causes heating. The rate of heat transfer is proportional to the magnitude of the current, while the direction of heat transfer is dependent upon the direction of the current.

HOW DOES THE PELTIER CHAMBER WORK?

The Peltier chamber in the 3450A is part of a closed-loop temperature control system. Figure 2 is a representation of this system. Controlling the magnitude and direction of the current through the Peltier junction allows control of the temperature in the chamber. The essential parts of the system are the controlled element (Peltier junction), the sensing element (Thermistor Rt) and the comparison and amplification elements (balanced bridge and cooler drive circuits).

The operation is as follows: the resistive bridge is balanced for a value of Rt corresponding to 43° C. A temperature deviation above or below 43°C produces a bridge imbalance through the thermistor, Rt. This imbalance is amplified by the cooler control amplifier and cooler drive amplifier. The cooler drive amplifier acts as a current source or current sump, depending upon the direction of the bridge imbalance. The current produced by the cooler drive amplifier causes the Peltier junction to heat or cool to correct the bridge imbalance.

WHAT COMPONENTS ARE LOCATED IN THE CHAMBER?

The component-mounting block serves as a mount for the reference power supply Zener and three dual FET's, one each for the input amplifier, the polarity amplifier and the ratio-percent amplifier. In addition, the sensing thermistor is also located on the block.

WHY USE A PELTIER CHAMBER?

First of all, using a Peltier chamber enables the 3450A to stabilize its temperature sensitive devices at a temperature (43°C) within the operating range (<50°C) of the instrument. This means that the problem of thermally isolating a high-temperature oven is avoided.

Secondly, the Peltier chamber has a lower thermal mass than the normal oven. With less to heat or cool, the chamber can reach stability conditions faster than an oven.

The Peltier chamber operating at 43°C stabilizes both the FET's and the reference Zener, eliminating the need for separate stability systems. The selection of 43°C as a stability temperature is based on the relative efficiency of the chamber as a heater or cooler. In the heating mode the Peltier junction in the 3450A is almost 100% efficient, while the cooling efficiency is only about 10%.

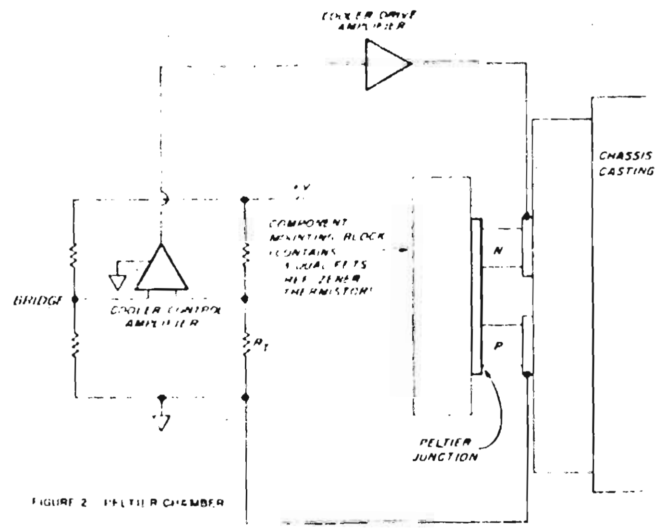


FIGURE 2 PELTIER CHAMBER

REFERENCES

The information above should be sufficient to answer most customer questions. Further, more specific information can be obtained from the following references.

1. Heaton, A.G., B. Sc. "Thermoelectric Cooling: Material Characteristics and Applications," Proceedings of the IEEE, Vol. 110, No. 7, July, 1963, p. 1277 - 1287.
2. Eichorn, R.L., "A Review of Thermoelectric Refrigeration," Proceedings of the IEEE, May, 1963, p. 721 - 735.
3. Wheeler, L.J., "The Design and Application of Peltier Coolers," Electrical Review, April 20, 1962, p. 663 - 669.

MANUAL CHANGES

(INSTRUMENT MODIFICATIONS)

MODEL 3450A MULTI-FUNCTION METER

Manual Part No. 03450-90003

Factory changes have been made to the 3450A at the following serial numbers:

953-01301

A53 R24 and Q11 have been changed to a matched set, Part No. 03450-69511. Some 953-013XX instruments and 956-01484 do not have this change.

956-01401

Wires to A56 and A57 assemblies now have connectors in the middle of the wires, rather than on the assemblies.
Gray and orange wires on A56: 03450-61612.
Gray wire on A57: 03450-61611.
Orange wire from A71 connector to A56: 03450-61613.

959-01501

A72 C6 is changed to 270 pF, 0140-0206.

959-01502 thru 05, 08, 09, 13, 14, 16-19, 21, 22, 26-29, 38, 40, 50, 52, 54-59, 61, 62, 64-70, 72, 74-78, 80-83, 85, 86, 88, 90, 94-96, 01600 and above.

A100 R7, R8 (51Ω 0686-5105) are added in series between the X and Y low input terminals and reeds K1B and K2B. See Page 7-45. CAUTION: Use the calibration adjustment procedure described in the Manual; do not use a digital voltmeter to adjust the Reference Voltage or Polarity AmpGain on Page 5-7.

959-01601

A53 R9 is changed to 20 kΩ, 0757-0449.

981-01701

The Percent-Amp Gain circuit on A56 assembly now controls the gain of the Percent Amplifier by changing the feedback resistance rather than the series resistance. The operation of the gain relays K25 through K27 is inverted; they close to determine the Percent Amp Gain. A56R7 does not change value for 50 Hz power line. See Page 2 for the circuit modifications.

A2 C15, C16 changed to 2.2 μF 0180-0197.

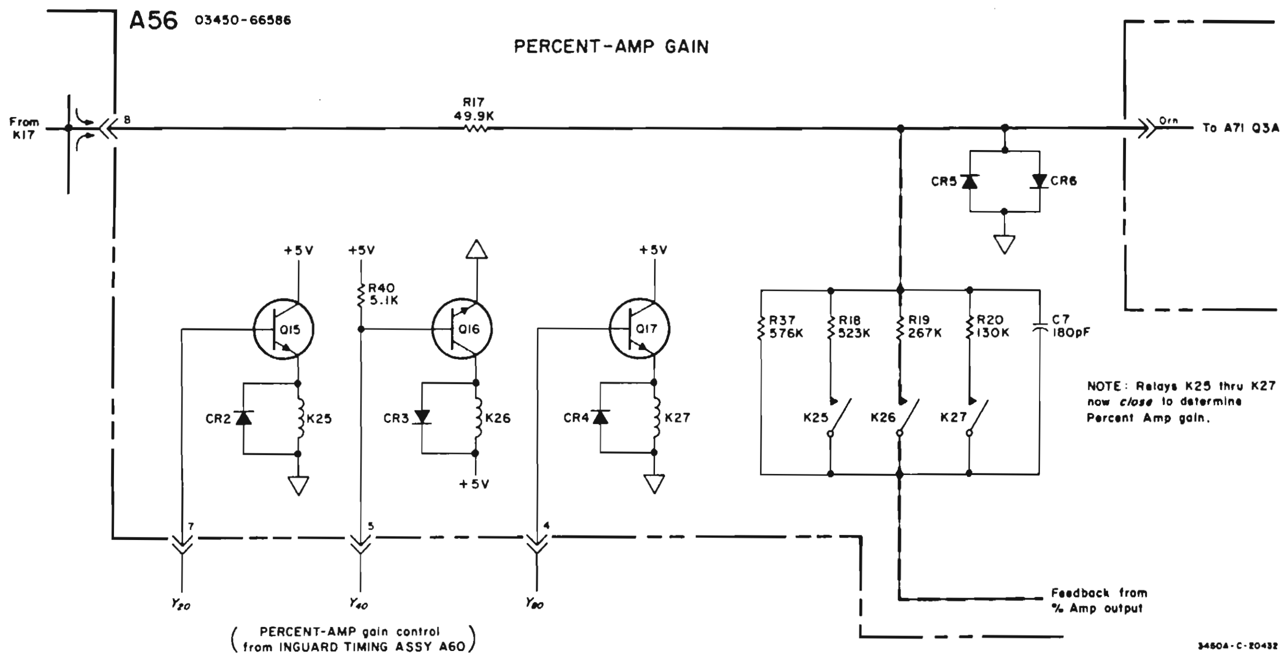
983-01801

A13 Decoding IC's changed to units that clamp the off-state output voltage to a low value. Further modifications are shown on Page 3.

988-01901

The GATE CONTROL and 6:1 DIVIDER circuits on A5 are changed as shown on Page 4.

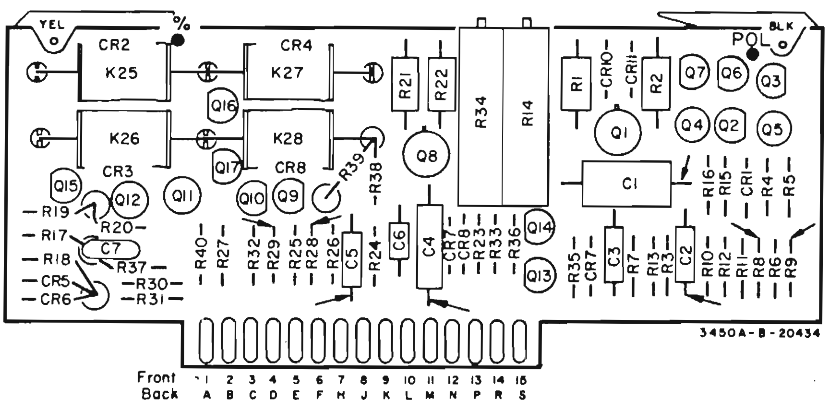
A56 03450-66586 installed in instruments 981-01701 and above.



A56

(03450-66586)

REV A



PARTS

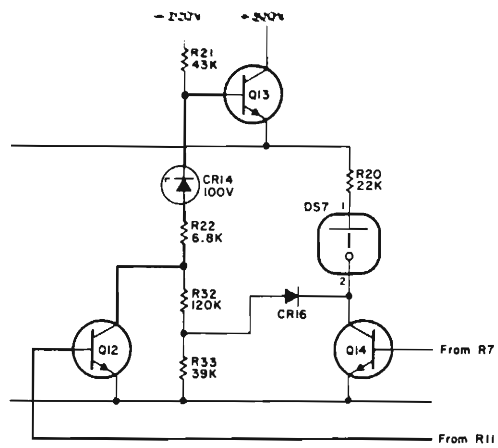
A56	Pol/% Amp Assy	03450-66586
C3	.0047 microfarad mylar	0490-0366
C7	180 pF 5%	0140-0147
K25 thru K28	Reed	0490-0366
R7	6.65 kilohms 1% 1/8 W	0698-3484
R10, R11	47 ohms 5% 1/4 W	0683-4705
R12	953 ohms 1% 1/8 W	0698-4125
R17	49.9 kilohms 1% 1/8 W	0698-3228
R18	523 kilohms 1% 1/8 W	0698-7802
R19	267 kilohms 1% 1/8 W	0698-4531
R20	130 kilohms 1% 1/8 W	0757-0468
	Post: terminal	0340-0037
	Bushing: terminal	0340-0039
	Insulator: feed thru	0340-0060

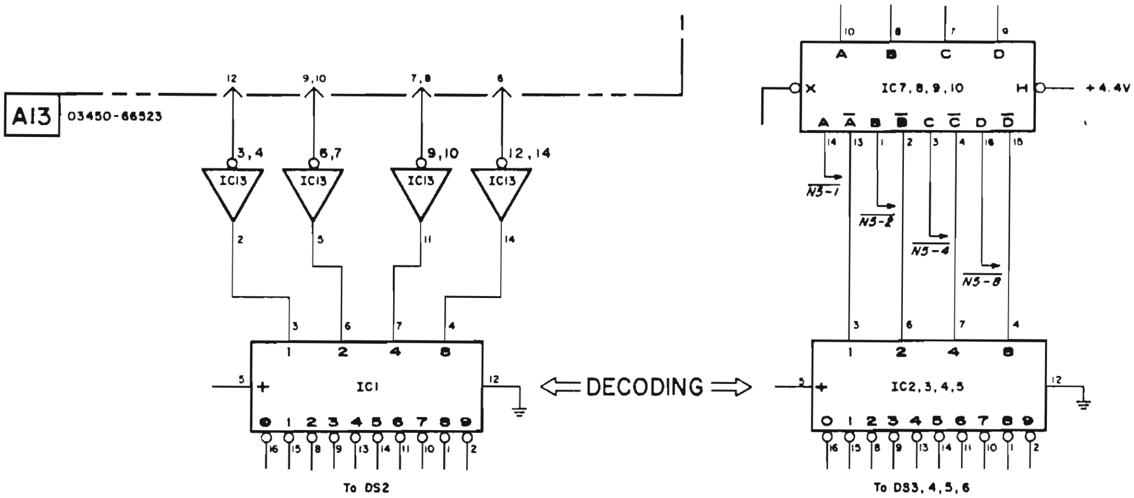
A13 03450-66523 installed in instruments 983-01801 and above.

PARTS

A13 Display Ass'y		03450-66523
IC1 thru IC5		1820-0426
IC13		1820-0303
R15 thru R20	20 kilohms	0686-2035
R23	deleted	
R32	120 kilohms	0683-1245
R33	39 kilohms	0683-3935
CR16	Si	1901-0025

DATA BLANK



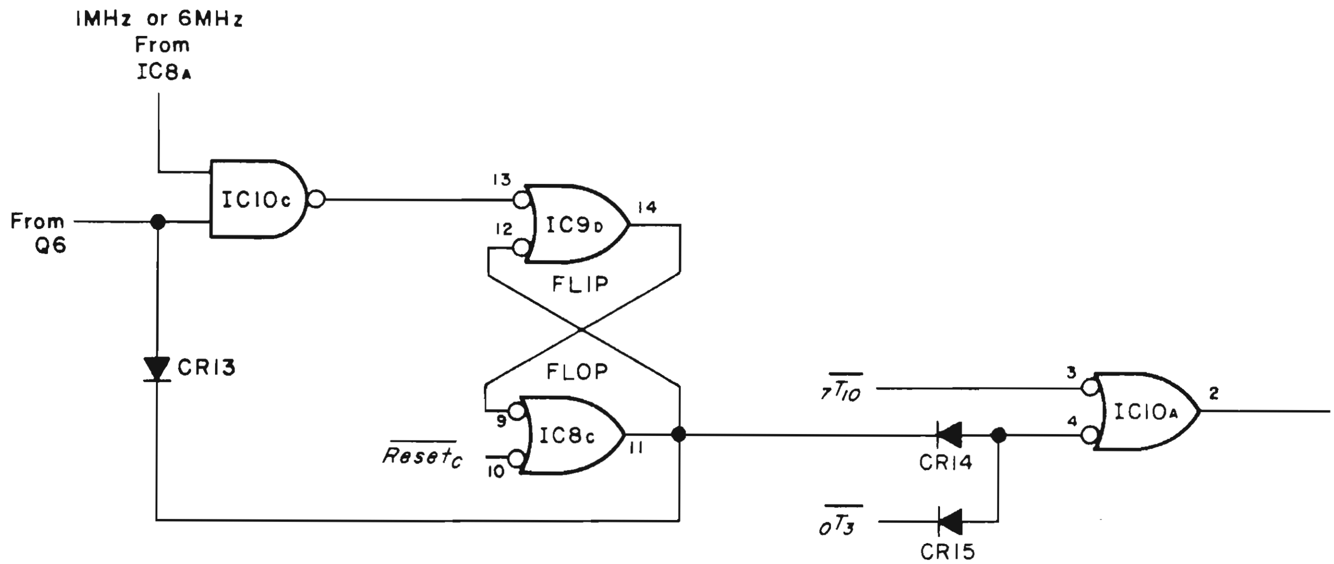


A5 03450-66505 REV E installed in 3450A's 988-01901
and above, and in some H50-3450A's 983-018XX.

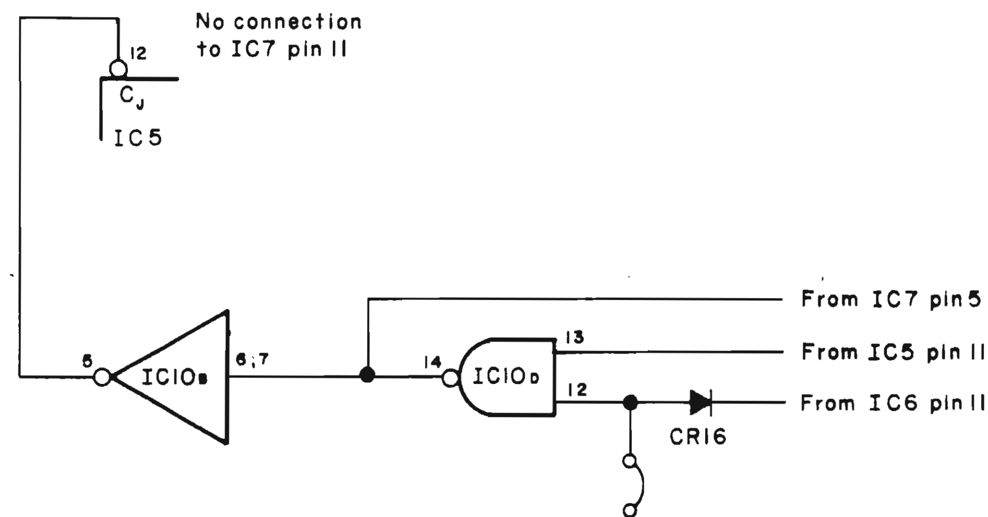
PARTS

IC10: 1820-0303
CR13-CR16: Germanium 1910-0016

A5 GATE CONTROL



A5 6:1 DIVIDER



IC10: 1820-0303
CR13-CR16: Germanium 1910-0016