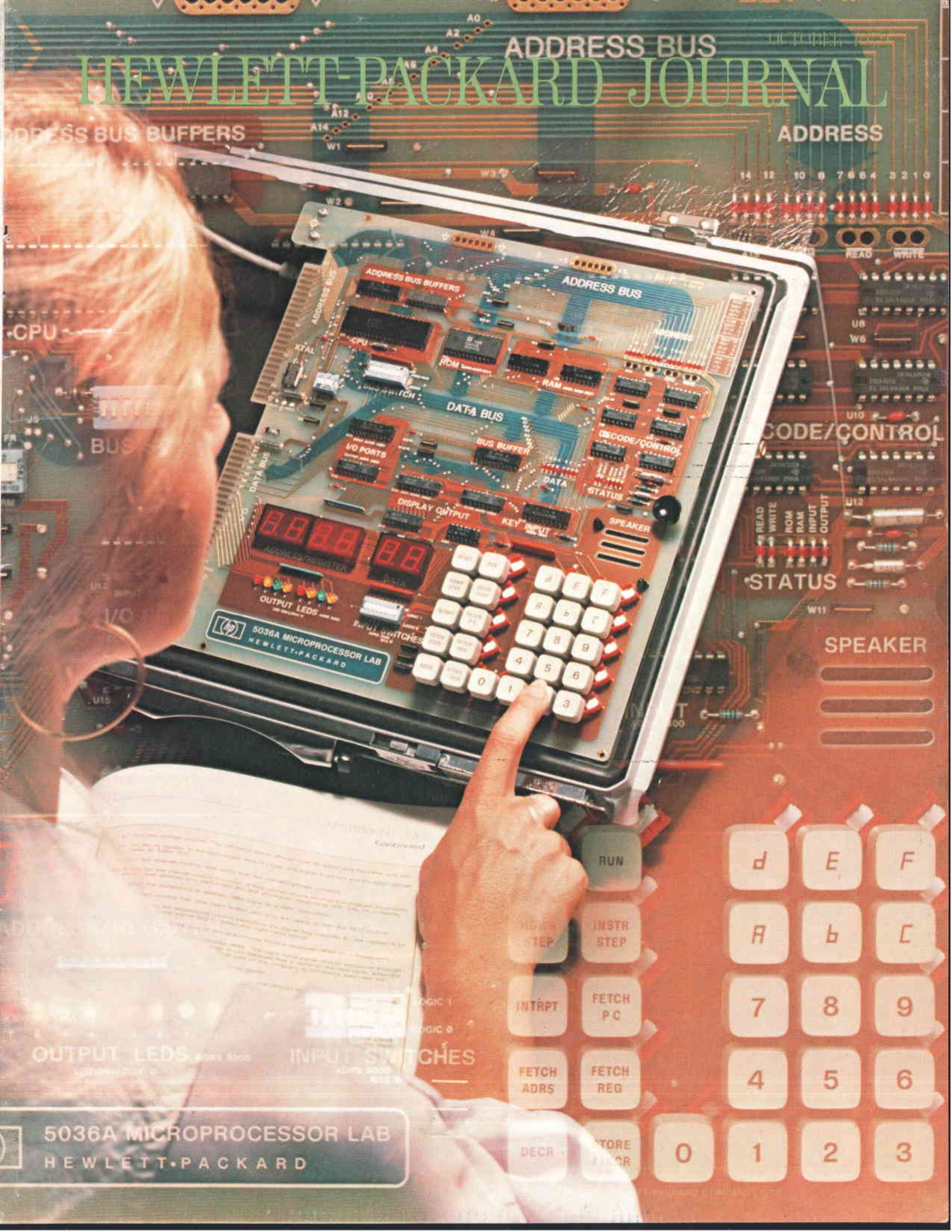
HEWLETT-PACKARD JOURNAL
ADDRESS BUS
ADDRESS BUS BUFFERS
ADDRESS
CPU
DATA BUS
I/O PORTS
BUS BUFFER
CODE/CONTROL
STATUS
DISPLAY OUTPUT
KEY INPUT
SPEAKER
OUTPUT LEDS
INPUT SWITCHES
5036A MICROPROCESSOR LAB
HEWLETT-PACKARD
READ
WRITE
ROM
RAM
INPUT
OUTPUT
RUN
INSTR STEP
INTRPT
FETCH PC
FETCH ADRS
FETCH REG
DECR

HEWLETT-PACKARD JOURNAL

Technical Information from the Laboratories of Hewlett-Packard Company

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Contents:

In this Issue:

Microprocessors—those tiny computers contained on single chips of silicon or silicon-on-sapphire—are contributing to our quality of life in more and more ways. They're in microwave ovens, stereo equipment, handheld calculators, electronic games, all kinds of industrial equipment, and some automobiles. With all these microprocessor-based products in service, some are bound to fail and need fixing. The product featured on this month's cover, Model 5036A Microprocessor Lab, is designed to teach service technicians how microprocessors work and how to troubleshoot microcomputer systems. It's the only microprocessor teaching aid currently available that emphasizes the latest troubleshooting and service methods. Besides service personnel, the microprocessor lab should be valuable to computer hobbyists and to technicians and scientists in many disciplines who want to learn about microprocessors. It's designed for home study or classroom use.

The article on page 9 is about the design of a new network analyzer, Model 8754A. Network analyzers tell system designers how electronic circuits and devices will behave as components of larger systems. For example, most network analyzers can measure how much of the power that goes into a device is transmitted and how much is reflected at various frequencies. Some network analyzers can measure the time relationship, or phase shift, between the input signal and the transmitted or reflected signal. Model 8754A measures both magnitude and phase over the frequency range of 4 to 1300 MHz. Its contributions include surprisingly good performance for its price, and surprisingly small size for a complete network analysis system.

The HP Interface Bus, or HP-IB, is an HP-pioneered method of putting together automatic test systems by connecting instruments to each other and to a computer or other controller. A new interface option now makes either of two HP logic state analyzers compatible with the HP-IB (page 18). Logic state analyzers have become important tools for designing and servicing computers and other digital systems. With the HP-IB connection, computer power can be added to these analyzers' capabilities, opening up many new possibilities.

Described on page 23 is a new kind of logic state analyzer, Model 1640A Serial Data Analyzer. This analyzer can tap into a serial data link and either monitor the data traffic or pretend to be a computer or terminal talking on the line. It's useful for troubleshooting data networks.

-R. P. Dolan

Microprocessor Lab Teaches Operation and Troubleshooting

This entry level course for home study or the classroom includes a microcomputer in a briefcase and a 20-lesson textbook.

by Barry Bronson and Michael Slater

THE PAST FEW YEARS have seen a flood of new products designed around microprocessors. This trend is expected to continue, with the microprocessor finding its way into not only more products but also a widening spectrum of applications.

While there are many educational alternatives available to teach engineers how to design microprocessors into products, little has been done to train the people who will have to repair these products. There are, for example, over 100,000 service technicians who will soon be confronting the microprocessor on a daily basis. Few of them have even a general understanding of microprocessors. One reason for this is that most courses on microprocessors stress design considerations, applications, and/or programming, but not troubleshooting or functional hardware operation for novices.

For years HP has been developing test instruments for the service market that help technicians and engineers troubleshoot electronic products. Serving this market, it became clear to us that there was a strong, perhaps urgent, need to bring the service industry up to speed on microprocessors. Drawing especially on our experience with the 5035T Logic Lab course on digital logic,[1] we established a project team with the goal of producing a similar product (both hardware and text) to fill the gap in microprocessor training.

The goal of the new product, Model 5036A Microprocessor Lab (Fig. 1), is to stress practical hardware and software concepts to provide students with a strong general understanding of how a microprocessor system works. The troubleshooting portion presents signature analysis and other specific troubleshooting tools and techniques so that the student will be prepared to use these important new tools to repair almost any microprocessor system. Special jumpers in the microprocessor lab hardware make it possible to introduce a variety of typical faults into the system. The student learns to troubleshoot these faults using the performance verification self-tests, diagnostics, and signature

Fig. 1. *Model 5036A Microprocessor Lab includes a keyboard-controlled microcomputer and a comprehensive textbook that contains both text and experiments.*

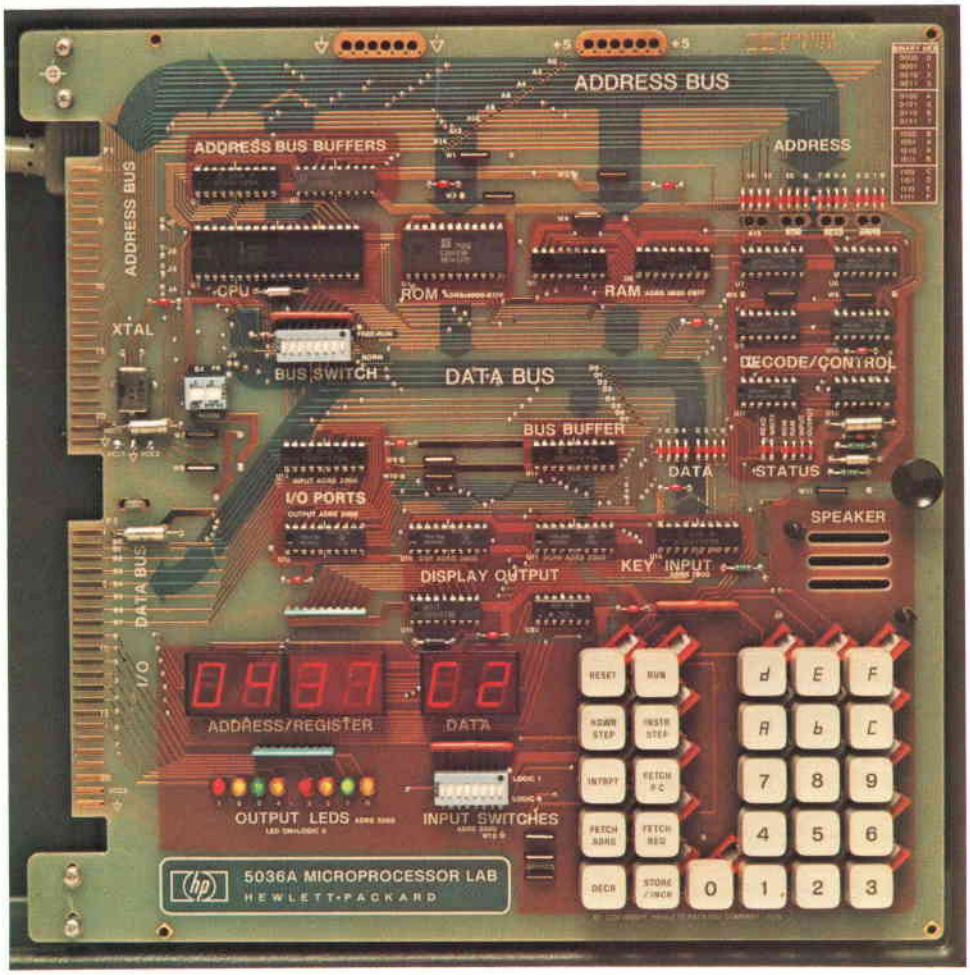


Fig. 2. *Graphics on the microprocessor board highlight function blocks and signal flow.*

analysis stimulus built into the product.

The course is intended to be self-instructional, like the 5035T Logic Lab, and to be an enjoyable experience for the student. The textbook is friendly and includes hands-on experiments using industrial-quality hardware.

The Hardware

At the time the 5036A Microprocessor Lab project was begun there were dozens of small single-board microcomputers available. For the most part, these boards were merely assemblies of parts that allowed a student to program particular microprocessor chips and see what they did. These boards could also be used to control an external circuit. The boards were generally sufficient to learn the basic programming and application of a particular microprocessor, but they were of little benefit in relating fundamental microprocessor design concepts to circuit hardware and system software, and of practically no benefit whatever in learning the techniques of hardware troubleshooting.

We also felt that many of these boards suffered from monitor program personalities that varied from unfriendly to hostile. Since the monitor provides the human interface to a microcomputer and controls the storing, modifying, running, and debugging of the user's programs, we felt that it was important to create a monitor with a friendly personality that was logical, consistent, and tolerant of a wide range of operator command sequences. To help the user get started with the course and to understand the general nature of the microprocessor lab, we have included demonstration programs permanently stored in the product to simulate such things as controllers and games.

In creating design goals for the hardware, we realized that what was needed was a complete, but very small microcomputer system, generalized to have as "classical" a structure as possible. Other aids to the student that we have included are:

1. A topology that is easily related to a microcomputer system block diagram and schematic
2. Liberal use of graphics to highlight function blocks and signal flow (Fig. 2)
3. The use of LED indicators on all main bus lines
4. A programmable speaker to provide an audible output. The speaker is used by the operating system to indicate errors, and can also be used by demonstration or user programs for signaling, playing music, and the like.
5. The ability to introduce hardware faults into the circuit to provide realistic troubleshooting examples. The student can introduce nondestructive electrical faults by means of removable jumper plugs located at various points on the microprocessor board. These faults simulate a variety of common faults that can be classified generally as either 1) stuck or open integrated circuit inputs or outputs or 2) broken or shorted board traces. Specific faults simulated are:

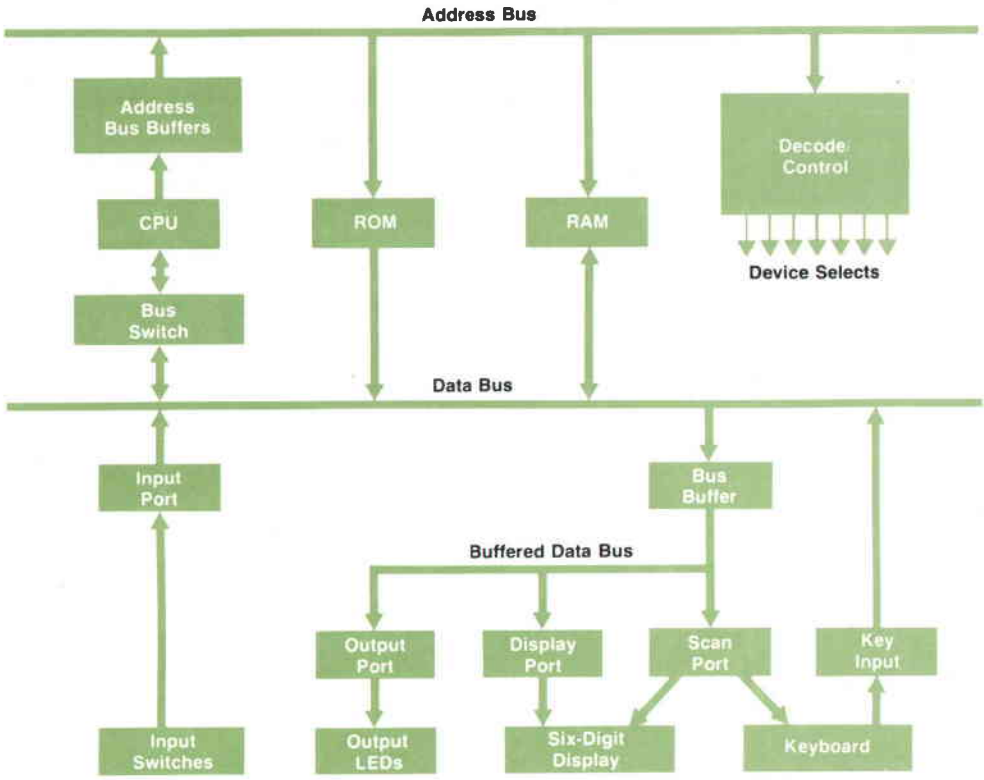


Fig. 3. *5036A microcomputer has a generalized, "classical" architecture.*

Shorted address bus lines
Bad ROM output line
Stuck ALE control signal
Bad RAM decoding
Bad address decoder
Bad memory protect circuit
Stuck Ready line
Stuck Hold line
Broken buffered data bus line
Shorted buffered data bus line
Open keyboard scan line
Shorted keyboard/display lines.

The Microprocessor

Implementing a classical microcomputer with real hardware meant that some compromise must take place, particularly in the case of the microprocessor. The Intel 8085A microprocessor was chosen for the microprocessor lab because it has a straightforward and typical architecture and very few unusual features, and requires only a minimal amount of support hardware. Also, the 8085A is a 5V-only system, can be used with general-purpose peripheral circuitry, and along with its predecessor the 8080, has substantial industry acceptance.

The major feature of the 8085A that we had to design around for instructional clarity was its multiplexed data and address buses. A simple eight-bit latch was used to separate these into two separate buses. Once this was done, generic chips could be used with the processor: static random-access read/write memories (RAMs), a read-only memory (ROM), eight-bit latches for output ports and eight-bit three-state buffers for input ports. Family-dependent large-scale integrated-circuit peripheral chips were avoided in the interest of preserving a generalized or classical system design. Fig. 3 is a block diagram of the 5036A Microprocessor Lab hardware.

Program Protection

Much consideration was given to protecting user programs stored in read/write memory (RAM). In typical microprocessor training products, relatively simple programming errors can result in the unintentional modification or even total destruction of the user's program.

To protect the user's program, the microprocessor lab has a hardware latch circuit that is automatically set by the monitor program whenever a student's program is run. This latch protects the first three-quarters of RAM program storage area from modification. The remaining quarter of the RAM is still available for data storage and the stack.

The microprocessor lab's power-up program performs a system self-test and memory initialization sequence when the system is turned on. In many microcomputer systems, common programming errors involving the microprocessor's stack pointer can cause the initialization program to execute, possibly wiping out the student's program. To prevent this, the microprocessor lab uses software interrogation of the status of the memory protect latch to determine whether the product is powering-up or executing a faulty program sequence. In the latter case an error message is displayed and the user's program is preserved. Additional memory protection is afforded by the use of two separate 5V power supplies, one for the memory portion of the microprocessor lab and the other for external circuit expansion. An accidental short on one supply does not affect the other; thus the risk of a program loss because of a hardware failure is reduced.

Single-Step Modes

Because the purpose of the course was to teach a basic understanding of both hardware and software, two types of single-step modes were implemented. The first mode, called hardware single-step, sets up the system to begin user program execution at a specified address and then stops all system activity at that address. The system can then be made to advance a single machine cycle each time the HDWR STEP key is pressed. Address, data, and control activities are monitored using LEDs on the address bus, data bus, and control lines. Thus the program instructions that result in data transfers, branches, and other system operations can be visually observed as the program is executed, one machine cycle at a time. At any point in this sequence, the user can return to the system monitor program by pressing RESET. This allows the user to examine and modify memory, register contents, or the program itself.

In the second single-step mode, called software single-step, an entire instruction is executed, regardless of the number of machine cycles, and then system control returns to the monitor program. Thus the program sequence can be observed instruction-by-instruction on the display. Branches, loops, and register and memory contents can be readily observed and modified at any point in the program.

The user can conveniently alternate between these two single-step modes at any point in the program.

As an additional aid for debugging programs, a software breakpoint feature is provided. To use this feature, the user stores a special breakpoint instruction code at strategic points in the program. Whenever the program reaches a breakpoint instruction, microprocessor activity transfers from the user's program back to the monitor program. The user can then examine and modify data in the registers and memory. Execution of the user's program can then be resumed from that point, if desired.

The Textbook

Among our major goals for the 5036A Microprocessor Lab coursebook were that it be complete and easy to read, and describe microprocessors from a practical point of view. The aim of the course is to enable the student to understand and troubleshoot microprocessor-based systems. The course is not intended to teach system design to digital design engineers.

Unlike many microprocessor texts, the new textbook, "Practical Microprocessors," takes a top-down approach. This approach starts by describing the big picture, and gradually works down to the details. Thus the course begins by describing microprocessor applications and overall system concepts. The hardware and software for typical systems is then described, with each chapter going into successively more detail.

Four lessons are devoted to troubleshooting techniques for microprocessor-based systems. A number of specialized tools are described, including logic probes, logic pulsers, current tracers, signature analyzers, and logic analyzers. General troubleshooting strategies are described and then demonstrated using the fault jumpers. This enables the student to gain actual troubleshooting experience with the guidance of the textbook.

This structure provides a clear, logical picture of microprocessor systems and their applications. It also allows a wide variety of students to adapt the course to their needs. For example, a student interested principally in troubleshooting microprocessor-based systems can omit the detailed software material and concentrate on the hardware and the troubleshooting chapters. On the other hand, a student whose main interest is software can skip the detailed hardware lessons and the troubleshooting section. Because of the course's top-down structure, both of these students will get a good overview of microprocessor hardware and software while learning the details of their particular areas of interest. A study guide, shown in Fig. 4, helps the student decide which lessons to study.

The book is divided into six sections, as shown in Fig. 4. Each section is divided into lessons, which are the main structural units of the course. There are twenty lessons in the complete course, each requiring 1½ to 2½ hours to complete. Each lesson is self-contained, enhancing the course's modular structure.

Each lesson consists of text and experiments intermixed. Instead of placing the experiments in a separate workbook, we have included them in the text at appropriate points to illustrate the concepts being discussed. Thus students should have a microprocessor lab available as they read the coursebook, since they will alternate between reading and performing experiments. Fig. 5 shows a typical page of text and Fig. 6 shows a typical page from one of the experiments.

At the end of each lesson is a summary, followed by a quiz. This allows students to review the material learned in the lesson, and then test themselves by taking the quiz. Answers to all quiz questions are in Appendix A. By

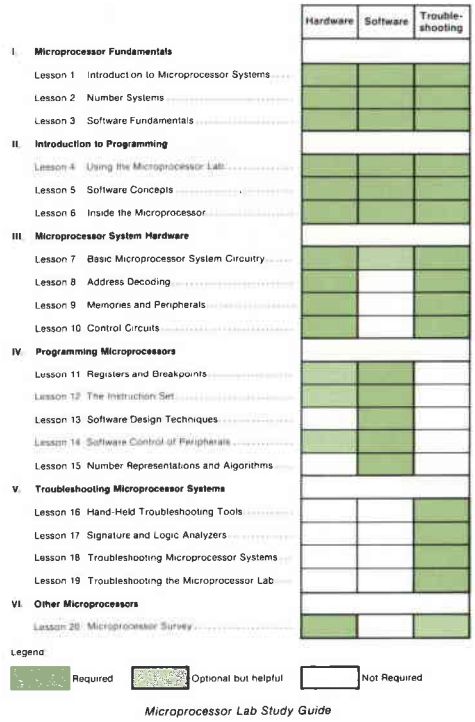


Fig. 4. *Study guide from textbook indicates which sections must be studied to learn microprocessor hardware, software, or troubleshooting.*

Input ports are connected in a similar manner, as shown in Figure 7-9. The output of the address decoder is ANDed with $\overline{READ}$ instead of $\overline{WRITE}$ to generate the port enable. The input port is an eight-line three-state driver which places the input signals on the data bus when enabled. The microprocessor can read the input signals by performing the read operation from the appropriate address. The processor then stores this data in one of its internal registers.

INPUT PORTS

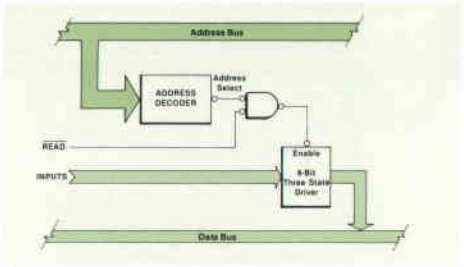


Figure 7-9. Input Data Placed on Data Bus Whenever Microprocessor Reads Address Assigned to Three-State Driver.

Suppose that an address decoder is required to control eight I/O ports instead of just one. Eight address decoders similar to the one in Figure 7-7 could be used, but there is a simpler method. Figure 7-10 shows an address decoder which generates select signals for addresses 3000, 3001, 3002, ..., 3007. For these eight addresses, only the three low-order address bits (A0, A1, and A2) of the 16-bit address are changed. The upper thirteen bits can therefore be decoded by a common circuit similar to the one in Figure 7-7. The output of this circuit is used to enable a decoder such as a 74LS138. This decoder then generates eight separate outputs, one for each possible combination of A0, A1, and A2. The decoder is disabled (all outputs are false) if the upper thirteen address bits

ADDRESS DECODING FOR MULTIPLE DEVICES

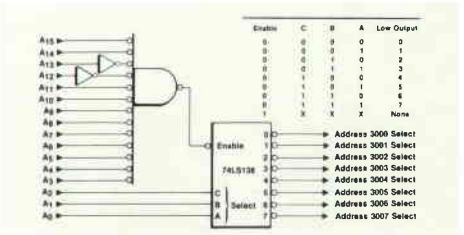


Figure 7-10. Decoder IC Provides Simple Way of Extending Number of Devices That Can Be Selected.

Fig. 5. *A typical page of text from the 5036A textbook.*

EXPERIMENT 16-3

Stimulus-Response Testing
Using the Probe and the Pulser

CONCEPT

This experiment demonstrates how the pulser can stimulate circuits in the μLab and how it can be combined with the logic probe to perform stimulus-response testing. The logic pulser injects a stimulus signal into a node, and the logic probe monitors the response of other circuit nodes in the signal propagation path.

HP 546A Logic Pulser

PROCEDURE

I. Tracing Logic Flow

A) Clear the μLab memory by turning the power off and then on. Fetch the first RAM address (0800) by pressing [RESET]. Press [SINGLE STEP] to enter the hardware single-step mode at address 0800. Verify that the bus LEDs are reading RAM data 00 at address 0800. The display is blank since the system has stopped.

B) Using the logic probe, verify logic 0 levels on the D0 data bus line and the RAM enable line (IC5-8). This tells you that the RAM is enabled and that the data present on its D0 output is 0. Now insert the probe into the D0 test hole (see Figure 16-10) and leave it there.

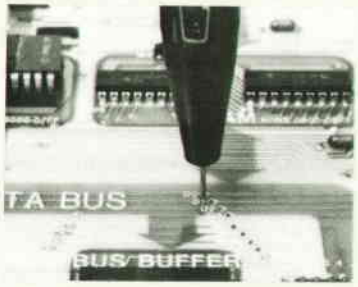


Figure 16-10. Logic Probe Inserted into D0 Test Hole.

Fig. 6. *A typical experiment page from the 5036A textbook.*

answering each quiz question and reviewing the material in the lesson as needed, the student can be sure of having learned the important points covered in that lesson.

A thorough set of appendices is also provided for reference material. A complete description of the 8085 instruction set is included as a programming reference. A comprehensive glossary of microprocessor and troubleshooting terminology is also provided. Other appendices include signature tables, demonstration and utility programs, a complete listing of the monitor program, directions for expanding the microprocessor lab hardware, and data sheets for the LSI (large-scale integrated) circuits used in the hardware. Finally, an annotated bibliography tells the student where to find additional information on microprocessor systems and troubleshooting techniques.

Refining the Text and Experiments

Since the course is designed for self-study, it was important to us that the text be clear and easy to understand, and that the experiments be as foolproof as possible. To help reach this goal, numerous people took the course at various stages of its development. These people were chosen to represent a cross-section of our intended students: service technicians, marketing engineers, technical instructors, supervisors, and design engineers were among the participants. In addition, several experts in the field reviewed the material for technical accuracy. As a result of the comments and criticisms that came from these reviewers, the coursebook went through three major drafts before its final form. This allowed us to tailor the course to the needs of various students, and to debug the text and experiments thoroughly. An experienced technical writer and an experienced book editor assisted in polishing the text.

Acknowledgments

Many people from diverse areas of specialty contributed to the design and development of the 5036A hardware and text. The original product concept was inspired by Bill Cardwell, and Gary Gordon helped refine this concept throughout the development process. Mechanical and industrial design was performed by Gary Schultheis and Kuni Masuda. Endless pages of text drafts were typed by Mia Aaron and Chris Hewett. Careful technical reviews were performed by Gary Sasaki and Ken Rothmuller, and Ed Dwyer and Barbara Carpenter contributed considerable writing and editing assistance. Bill Kampe and Ray Morgan managed the production of the book, which was designed by Jodi Smith. Irene Chan was the chief illustrator. Bruce Hanson provided marketing expertise, and the smooth transition of the product from the lab to production was assisted by Roy Criswell, Dick Harris, Bill Feeley, and Rich Endo.

Reference

1. J.A. Marrocco and B. Bronson, "A Quality Course in Digital Electronics," Hewlett-Packard Journal, November 1974.

SPECIFICATIONS
HP Model 5036A Microprocessor Lab

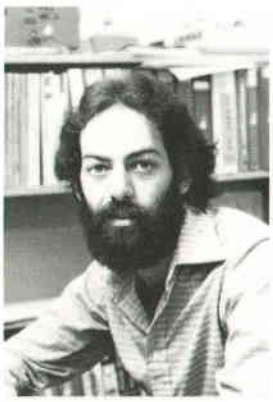
TIME BASE OUTPUT: 2 MHz ±0.05%, crystal controlled
I/O PORTS:
OUTPUT DRIVE: Each output will drive a minimum of one LS TTL load.
INPUT LOADING: Each input equals no more than 3 LS TTL loads.
POWER SUPPLY:
SUPPLY 1: 5V dc ±10%, 250 mA available for external circuitry.
SUPPLY 2: 5V dc ±10%, 175 mA available for external circuitry.
POWER REQUIREMENTS: 100/120/220/240V ac ±10%; 48 to 66 Hz line; 50 VA maximum.
OPERATING TEMPERATURE: 0-55°C.
DIMENSIONS: 514.4 mm L × 371.5 mm W × 177.8 mm H (20.25 × 14.625 × 7.0 in).
WEIGHT: Shipping: 7.7 kg (17 lb). Net: 6.73 kg (14 lb 10 oz).

Supplemental Operating Characteristics

MICROPROCESSOR: 8085A
ROM: 2316E; 2K bytes.
RAM: Two 2114/4045's; 1K bytes.
DISPLAYS:
ADDRESS/REGISTER DISPLAY: 4 digits; 7-segment LED displays.
DATA DISPLAY: 2 digits; 7-segment LED displays.
OUTPUT PORT: 8 LED's; one per output line.
ADDRESS BUS: 16 LED's; one per line.
DATA BUS: 8 LED's; one per line.
STATUS LINES: 6 LED's; one per line.
I/O: 8-bit latched output port with LED indicators. 8-bit input port with DIP switch.
SIGNATURE ANALYSIS:
8-bit DIP switch used to disconnect MPU data lines from data bus.
"SA Loop" switch selects test loop program.
"Free-Run" switch selects free-run test mode.
TROUBLESHOOTING JUMPERS: 12 user-programmable fault jumpers on circuit board simulate various hardware faults.
TROUBLESHOOTING DOCUMENTATION: Troubleshooting tree, block diagram, schematic, signature tables provided to determine faulty nodes.
RECOMMENDED ACCESSORIES:
Model 5024A Troubleshooting Kit (545A Probe, 546A Pulser, 547A Current Tracer, and Vinyl Case).
Model 5004A Signature Analyzer.
PRICES IN U.S.A.:
5036A, including microprocessor system, briefcase with integral power supply, and one copy of course book, "Practical Microprocessors", $800. 5024A, $625. 5004A, $990.
MANUFACTURING DIVISION: SANTA CLARA DIVISION
5301 Stevens Creek Boulevard
Santa Clara, CA 95050 U.S.A.

Barry Bronson

Project leader for the 5036A Microprocessor Lab, Barry Bronson has been with HP since 1971. He was the principal hardware designer of the 5036A and co-author of "Practical Microprocessors." A graduate of the University of California at Los Angeles, he received his BS degree in engineering in 1970. His MSEE degree is from Stanford University (1975). Barry was project leader for the 546A Logic Pulser and is named inventor on a patent on that product. He was also design engineer for the 5035T Logic Lab, and has developed several automatic production test systems. Born in Los Angeles, California, Barry is married, has two daughters, and lives in Saratoga, California. He spends his spare time teaching a class in microprocessor design at the University of Santa Clara, pursuing his interest in electronic projects, photography, and stereo, and working on miscellaneous projects for the family's recently acquired home.



Michael Slater

A native of Los Angeles, California, Michael Slater came to HP in 1977 after receiving his BS degree in electrical engineering/computer science from the University of California at Berkeley. He contributed to the hardware design of the microprocessor lab and is the principal author of "Practical Microprocessors." Two evenings a week, he teaches continuing-education classes in microprocessor system design and design for serviceability. Now a resident of Menlo Park (with his two cats), Michael's favorite leisure activities are organic gardening and backpacking.

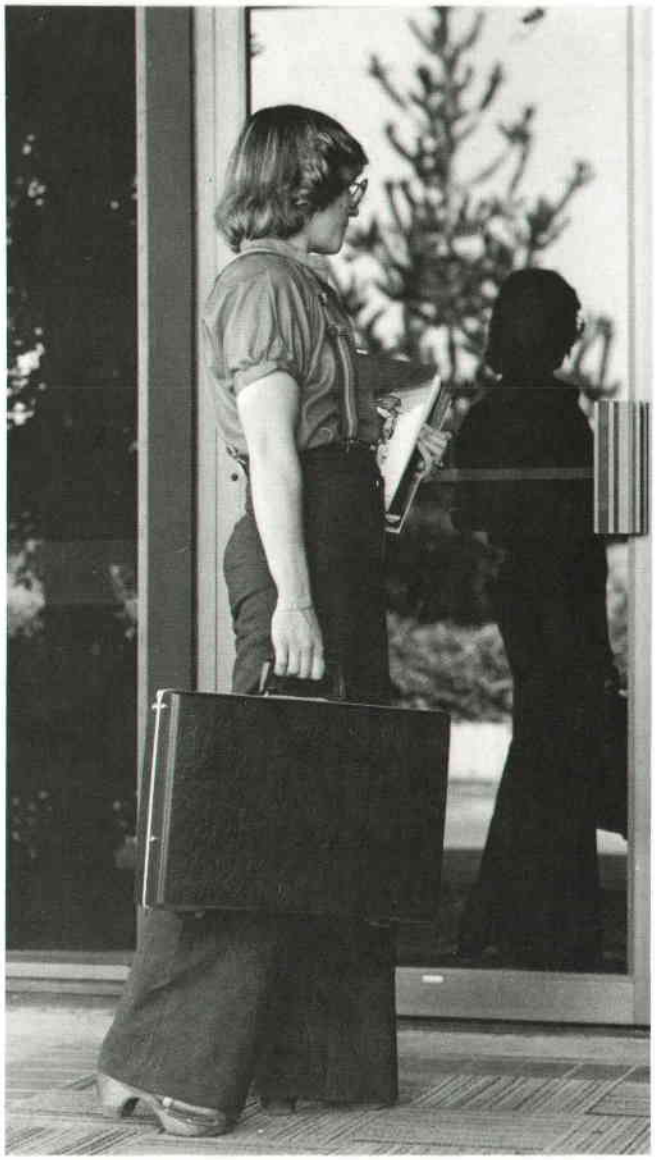


Fig. 7. *The microprocessor lab is contained in a briefcase that also has space for logic probes.*

An Economical Network Analyzer for the 4-to-1300-MHz Frequency Range

This compact, moderately-priced instrument has a built-in sweeping source and a two-channel receiver that enables simultaneous swept measurements of magnitude ratio and phase angle as well as measurements of absolute power and reflection coefficient.

by James R. Zellers

MEASUREMENTS OF SIGNIFICANT NETWORK characteristics—such as gain, phase shift, and input/output impedance—are essential in designing a circuit to meet performance objectives. Swept displays of these parameters as a function of frequency provide lucid insights into overall circuit behavior and make the effects of adjustments or other circuit alterations immediately visible. Network analyzers provide this kind of display.

The alternatives available for swept network measurement in the HF-to-UHF range have generally been classified into two types. The most common type is the amplitude-only measurement system using crystal detectors to sense the RF power. These systems tend to be compact, easy to operate, and relatively inexpensive but their dynamic ranges have been limited to about 60 dB and their broadband inputs are sensitive to the harmonics of the driving source. Tuned-receiver systems, on the other hand, measure magnitude and phase accurately over dynamic ranges up to 100 dB, but they have tended in the past to be complex and expensive.

Model 8754A, pictured in Fig. 1, is a new, cost-effective network analyzer for RF network measurements in the 4-to-1300-MHz frequency range. It is an all-in-one instrument that includes a swept signal source, a dual-channel, tuned, tracking receiver, and a CRT display—all in a 5¼-inch-high cabinet. It performs measurements of magnitude ratio, phase, absolute power, and polar reflection over an 80-dB dynamic range. Its accuracy, versatility, and ease of

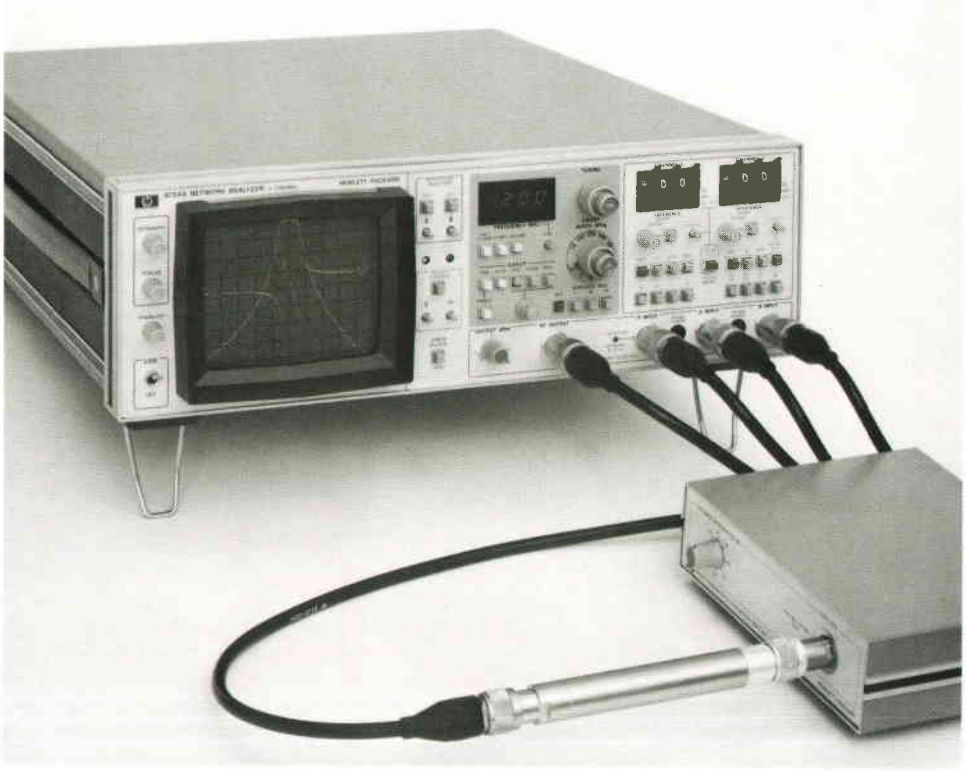


Fig. 1. *Model 8754A Network Analyzer makes swept measurements of absolute power, gain/loss, phase, and reflection coefficient over a frequency range of 4 to 1300 MHz. Dual-channel operation permits display of two parameters simultaneously in the rectilinear display mode, or magnitude and phase angle in the polar display mode.*

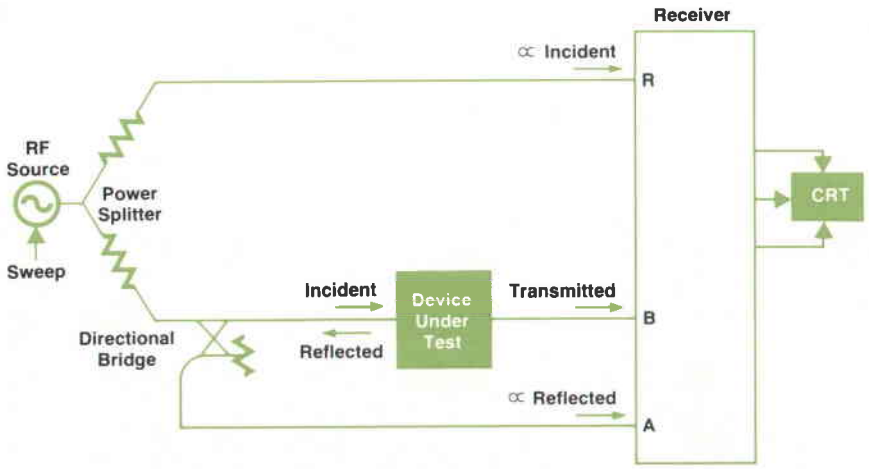


Fig. 2. *Basic network analyzer measures device characteristics by comparing the signal entering the device (incident) with the signals leaving the device (reflected or transmitted) and displaying the difference in dB or degrees.*

use suit it to a broad range of laboratory and production applications while its compact size permits its use in the field for measurements on devices such as antennas. Although its cost approaches that of the moderately-priced amplitude-only instruments, its phase-measurement capability, 80-dB dynamic range, and better than −80 dBm sensitivity, are comparable to more expensive network analyzer systems.

The built-in 4-to-1300-MHz source has flexible sweep-frequency capability with less than 7-kHz residual FM, and with output power calibrated to +10 dBm. The user may select either a START or CENTER frequency and the frequency is indicated on a 3½-digit LED display. It can sweep over the full 4-to-1300-MHz frequency range or provide narrower sweep widths ranging from 1 MHz to 1 GHz. It also has a CW mode. Crystal-controlled markers provide accurate frequency calibration.

The receiver has three RF inputs and two independent display channels so that two parameters, such as gain and phase, can be viewed at the same time (on alternate sweeps) with a single test set-up. Each channel has precision offset and measurement-range controls. Equalization of differing RF cable lengths in the measurement channels is possible over a 16-cm range with built-in adjustable length compensation. A polar display mode is also provided for impedance measurements.

Since this instrument is capable of a broad range of measurements, a number of accessories have been developed to give the user flexibility in measurement setups. These provide the interconnections required for almost any measurement need in both 50Ω and 75Ω systems. For example, Fig. 2 shows a typical test set-up for measuring the transmission gain or loss (B/R) in a filter, amplifier, or attenuator, the phase shift through the device (PHASE B/R), and the reflection coefficient (A/R). The external elements required for this measurement (power splitter, directional bridge, and suitable attenuators and pads) are provided in the Model 8502A/B Transmission/Reflection Test Sets. Also available are a three-way power splitter that enables the response of a device to be compared to a standard, an s-parameter test set that allows transmission and reflection measurements on both ports of two-port devices, transistor fixtures for the s-parameter test set, and high-impedance probes for in-circuit tests (power for active probes is provided at the front panel).

The measurement capabilities of Model 8754A are illustrated by the displays shown in Fig. 3. The display at left shows the transmission loss and input match of a 1-GHz high-pass filter over a greater-than-80-dB dynamic range. Note that the −30-dB source harmonics have negligible effect on the dynamic range, a result of using a narrow-band tuned receiver. The display at right is a polar display of the reflection from the input of a transistor amplifier over a 4-to-1300-MHz range. For this measurement, a Smith chart overlay (supplied with the instrument) is installed on the face of the CRT to permit direct readout of R+jX.

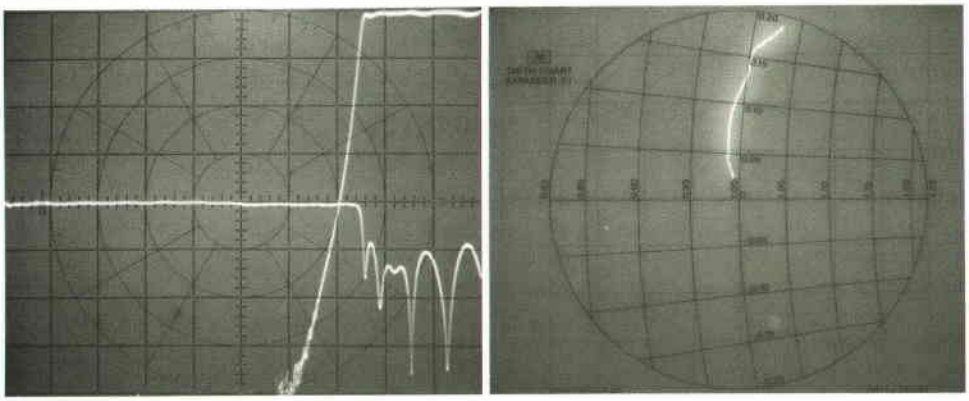


Fig. 3. *Display at left shows the transmission characteristics of a 1-GHz high-pass filter measured over a frequency range of 4 to 1300 MHz by Model 8754A. The vertical scale is 10 dB/div. The display at right was made in the polar mode with a Smith chart overlay installed on the CRT. This shows the input impedance of a transistor amplifier to be near 50Ω at low frequencies, becoming increasingly inductive at the higher end of the 4-to-1300-MHz measurement range.*

Making a Measurement

When measurements are made with the 8754A, the TUNING control sets either the START or CENTER frequency of the frequency sweep, as selected by the operator, and the SWEEP WIDTH control determines the width of the frequency sweep. The LED frequency display, derived from the tuning voltage, is easily calibrated to the crystal markers by using the FREQUENCY CAL control.

To prepare the instrument for magnitude and phase measurements, a reference line is first established on the CRT graticule by pressing the REFERENCE POSITION pushbutton for the selected channel. As shown in Fig. 4, this disconnects any signal input to the CRT. The REFERENCE POSITION control may then be used as a vertical-position control to place the displayed horizontal line where desired on the graticule, usually the top or center graticule line. This is the position around which the display will expand. With the REFERENCE POSITION pushbutton released, absolute power measurement may now be made by reading the value directly from the CRT. For higher precision, the procedure is

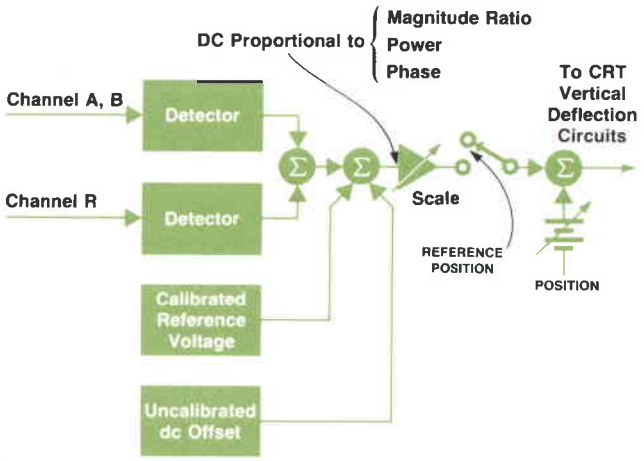


Fig. 4. *Offsets added to the measurement voltage enable calibration of the CRT graticule for direct readout of power, magnitude ratio, and phase.*

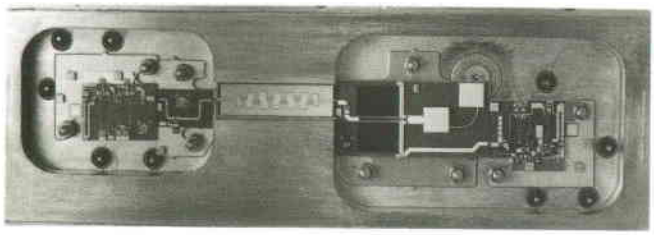


Fig. 5. *Thin-film source has two varactor-tuned oscillators installed in separate cavities to avoid potential injection-lock problems. Between them is a modulator (in the left cavity), a 5-GHz low-pass filter (in the connecting channel), and a mixer.*

to use the REFERENCE lever switch to bring the signal as close as possible to the reference line (the lever switch adds a calibrated offset to the displayed signal). The signal level may then be determined with three-digit resolution by adding the two-digit lever switch setting to the value of the residual displacement of the signal from the reference line, as determined by interpolating between the CRT graticule lines.

For ratio measurements, a calibration run is made with the measurement circuit connected without the test device in the circuit. With the REFERENCE lever switch set to zero, the REFERENCE OFFSET control is used to bring the displayed line to the reference line. The test device is then connected and the measurement made and evaluated with the aid of the lever switch and graticule interpolation.

Further conveniences for high-resolution measurements can be obtained by using the 8754A with either the Model 8750A or 8501A Storage/Normalizer.[1] These devices can store the results of a calibration sweep in their digital memories and then subtract the calibration trace from subsequent measurements to present a normalized trace. Fast repetitive readouts from their memories assure bright, flickerless displays even when sweeps are made very slowly. An interface connector for these instruments is provided on the rear panel of the 8754A.

RF Source

Extensive use of thin-film microelectronics enables the

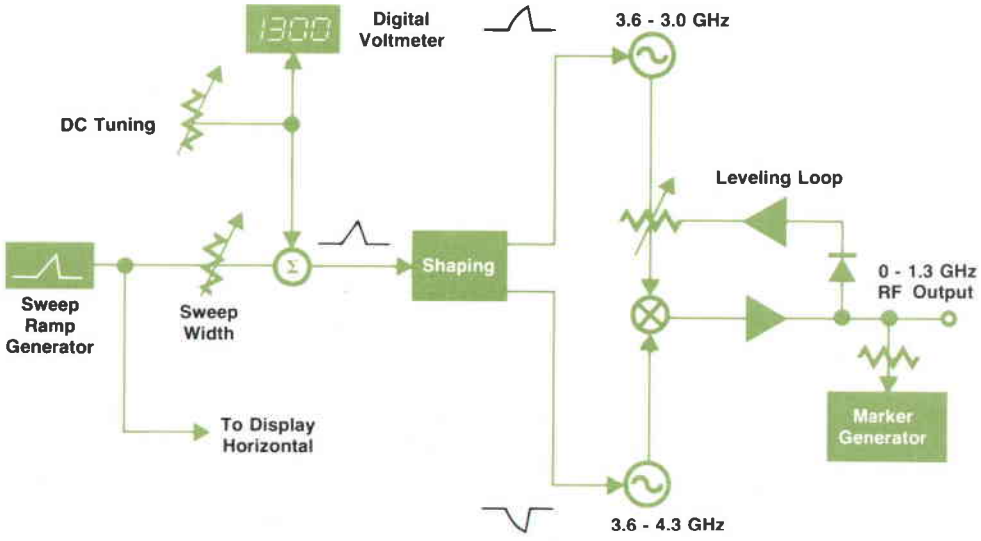


Fig. 6. *The RF output is a difference frequency derived from the two varactor-tuned microwave oscillators.*

Model 8754A to achieve the objective of high performance at moderate cost in a small package. For example, the source (Fig. 5) uses two thin-film varactor oscillators that have a residual FM (7 kHz) approaching that of YIG sources but that are considerably smaller and lower in cost.

As shown in the block diagram of Fig. 6, one varactor oscillator sweeps up in frequency from 3.6 to 4.3 GHz and the other sweeps down from 3.6 to 3.0 GHz. The difference of the two frequencies is taken from a mixer and amplified for the output. A wideband sweep is thereby obtained from two relatively narrowband oscillators.

Each of the varactors has a nonlinear frequency-versus-tuning-voltage characteristic. A 13-point diode shaping network modifies each tuning-voltage ramp so the RF output frequency is always linear within ±2 MHz. Overall stability is not degraded by the shaping networks and is typically within 300 kHz/°C or 100 kHz/hour after a half-hour warm-up.

Markers for Frequency Calibration

The LED FREQUENCY display and the SWEEP WIDTH control may both be calibrated with the aid of markers that occur at harmonics of 1, 10, or 50 MHz. The basic reference is a 50-MHz crystal oscillator that is accurate within 0.01%. A programmable divider yields a 1, 10, or 50-MHz square wave, according to front-panel selector pushbuttons, that is shaped into harmonic-rich narrow pulses by a step-recovery diode. The pulse train is mixed with a sample of the RF output signal producing a zero-beat "birdie" whenever the RF output frequency is equal to one of the pulse-train harmonics.

The birdies are shaped into clean-looking rectangular pulses by the digital detector shown in Fig. 7 and added to the video waveform applied to the CRT display for rectilinear displays, or to the Z-axis signal to give brightened pips on polar displays. The width of the marker pulses is controlled by the sweep width selector so they are always relatively narrow for most sweep widths. The calibrated marker frequency occurs at the center of each marker pulse

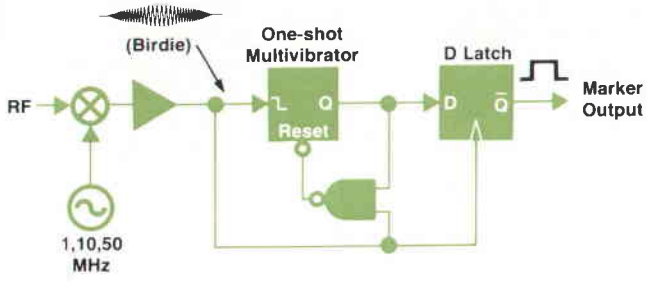


Fig. 7. *Pulse-width discriminator generates a marker pulse whenever the RF frequency sweeps through a harmonic of the reference. The negative-going edge of the amplified mixer output (birdie) triggers a one-shot multivibrator and the positive-going edge clocks a D flip-flop. When the birdie frequency approaches zero, the one-shot pulse will have cleared by the time the next positive transition occurs, and a zero will be latched into the flip-flop. A marker is then generated. When the birdie frequency is high (far away from zero beat), the one-shot will not have cleared when the flip-flop is clocked and no marker pulse results. In this case, the NAND gate resets the one-shot.*

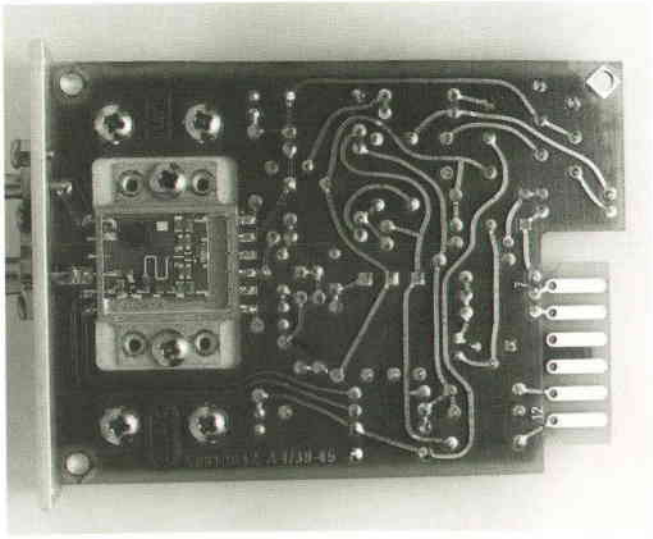


Fig. 8. *Thin-film sampler is housed in a low-cost stripline package mounted to the printed-circuit board containing the preamplifier circuits.*

on the display.

Alternatively, an external marker frequency may be applied at a rear-panel connector. This will appear on the display as a single marker at the position corresponding to the frequency of the marker. Also, when the instrument is sweeping the full 4-to-1300-MHz frequency scan, a single marker occurs at the frequency selected by the TUNING control. This then becomes the START or CENTER frequency on narrower sweeps.

Swept Vector Voltmeter Receiver

The receiver uses the sampling technique to down-convert the RF at each of its three inputs to a 1-MHz IF. The samplers (Fig. 8) achieve −80-dbm sensitivity, which is about midway between the sensitivities of simple diode detectors and the more expensive heterodyne-mixer systems. Frequency response is within ±0.3 dB. A block diagram is shown in Fig. 9.

The basic sampler design was derived from the principles used in the Model 8405A Vector Voltmeter.[2] Each RF input is sampled by a four-diode gate that is switched on by repetitive 300-ps pulses. Diode isolation networks in each pulse line (series diodes biased off, shunt diodes biased on) prevent one RF channel from interfering with another.

Each sample is stored on a holding capacitor until the next sample occurs. The sampling rate is automatically controlled so each sample occurs at an earlier point on the waveform during a subsequent recurrence of the waveform. Hence, over a period of several waveform cycles, the waveform is reconstructed on the holding capacitor. However, the reconstructed waveform has a much lower frequency, which makes it possible to perform precision phase measurements. The three pulse trains are phase-coherent so the IF signals in all three channels have the same phase relationships as the RF inputs.

The sampling effect is analogous to a harmonic mixer that mixes the RF input with a harmonic-rich pulse train to produce an output at a frequency $f_{RF} - nf_{pulse}$, where n is a

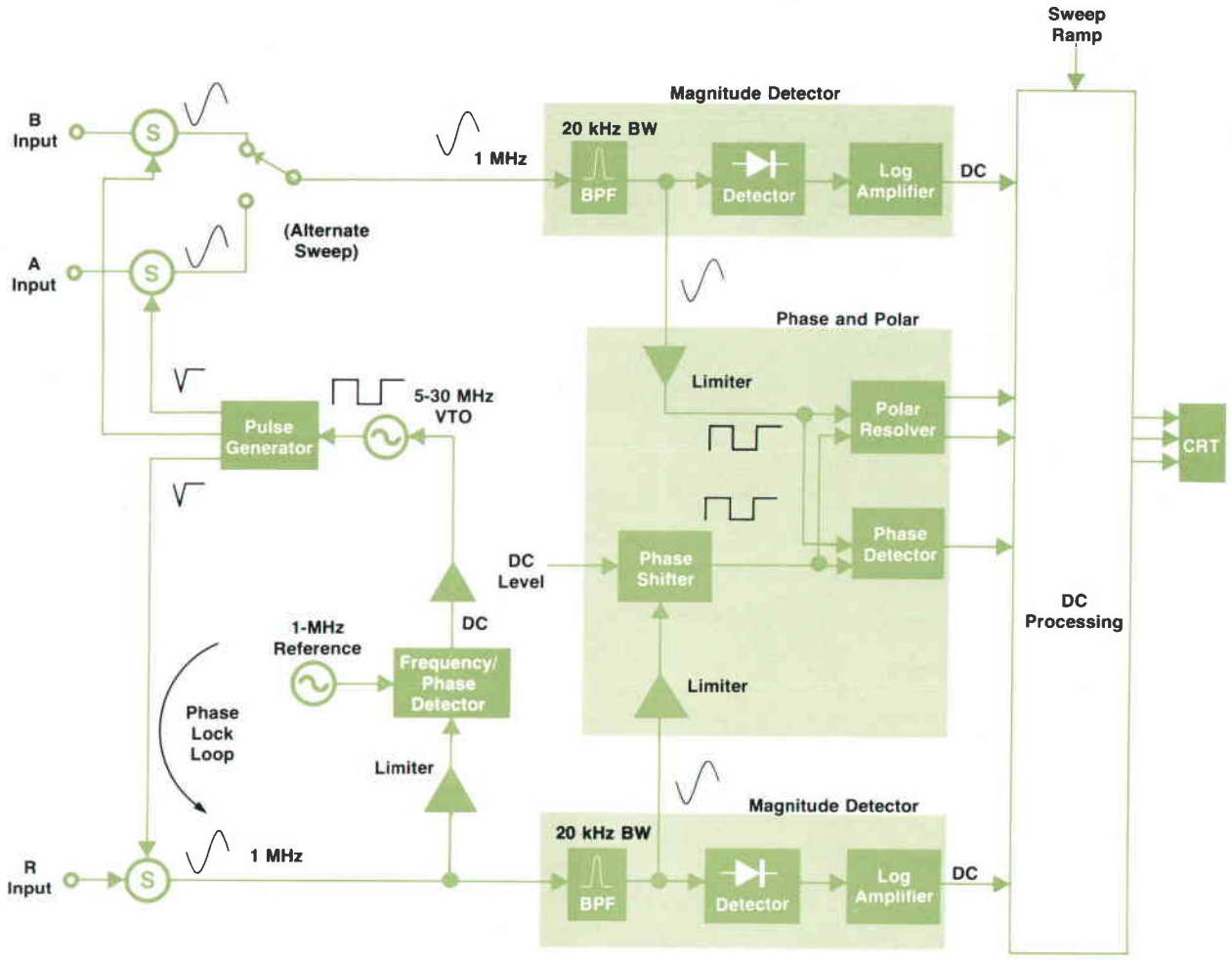


Fig. 9. *Three-input receiver has a reference channel (R) for phase and magnitude-ratio measurements and a time-shared channel. The alternate sweep switch allows two quantities, applied through the A and B inputs, to be displayed simultaneously. All three inputs are down-converted by samplers serving as mixers.*

harmonic number.

The pulses that drive the three samplers are generated by a step-recovery diode driven by a 5-to-30-MHz voltage-tuned oscillator (VTO). A 1-MHz intermediate frequency at the sampler outputs is maintained automatically by a phase-lock loop that controls the VTO frequency. A frequency/phase detector compares the output of the sampler in the R channel to a 1-MHz reference (Fig. 9). The resulting error voltage tunes the VTO as the RF input signal sweeps such that one of the VTO's harmonics is 1 MHz higher than the RF signal.

A limiting amplifier preceding the frequency/phase detector allows the system to operate with any R-signal amplitude within a range of 0 to −40 dBm. The use of two integrators (not shown in Fig. 9) in the feedback loop results in a third-order system that is able to maintain the 1-MHz IF within ±1 kHz as the RF signal sweeps at rates in excess of 130 MHz/ms.

Continuous Trace

The VTO phase-lock system works over an RF sweep range of 1½ octaves. There are, however, many times when wider sweeps are desired. In these cases, the analyzer functions in a multiband mode, switching to higher harmonics of the VTO so sweeps can be continued beyond the 1½-octave limit. Digital logic controls the VTO operation, RF sweep, and CRT display to present a continuous trace that has no gaps or transients where bandswitching occurs.

Before a sweep starts, the VTO is tuned to approximately 8 MHz and the tuning adjusted to phase lock one of the VTO harmonics to the RF start frequency. The sweep then starts, and the VTO tracks the RF signal until the VTO frequency reaches 30 MHz. When that occurs, the sweep stops, the display is held and blanked, the VTO is retuned to 8 MHz, and it is allowed to phase lock on a higher harmonic. The sweep then continues with the CRT unblanked until the VTO again reaches 30 MHz, and the cycle repeats. For a 4-to-1300-MHz full-band sweep, four such lock points occur.

The lock points are practically invisible on the CRT (Fig. 10) because the sweep is back-stepped about 4% during the VTO retuning interval. When the sweep resumes, the CRT remains blanked until the sweep reaches its old value. Thus, display transients associated with an abrupt start of a

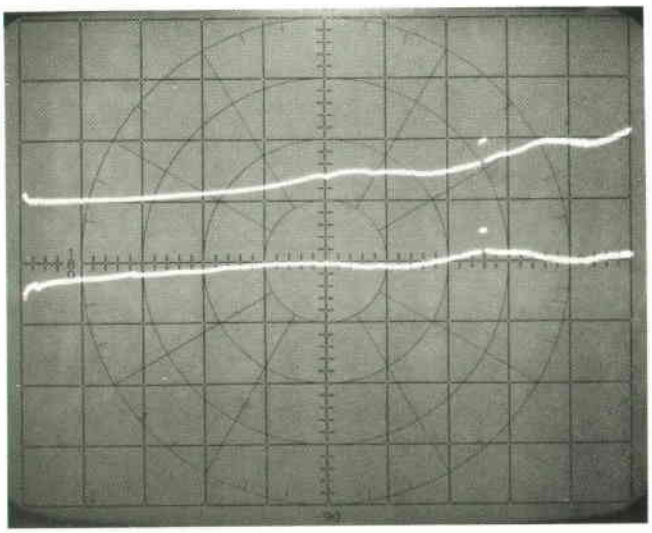


Fig. 10. *Wide 4-to-1300-MHz-sweep display of magnitude (upper trace, 0.25 dB/div) and phase (lower trace, 2.5°/div) shows no transients where the four frequency relock points occur. The tunable marker is positioned at 1 GHz.*

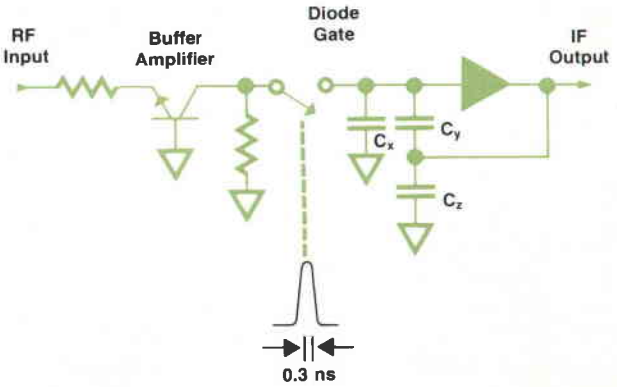


Fig. 11. *Sampling circuit uses a positive feedback loop around the amplifier to boost the charge on holding capacitor C_x to full value.*

sweep are blanked.

One problem with some wide-sweeping sampling systems is the change in amplitude response caused by a change in the sampling frequency. This is a result of series resistance in the sampling circuit that prevents the holding capacitor from fully charging to the new value of the RF signal during the short sampling pulse. Thus, the IF output amplitude drops as the sampling rate drops. This appears on the display as an abrupt discontinuity at harmonic relock points.

In the Model 8754A, a feedback circuit prevents this from happening by boosting the charge on the holding capacitor between samples. A circuit diagram is shown in Fig. 11. Because of its limited bandwidth, the amplifier does not respond to a new value on holding capacitor C_x during the sampling pulse, but responds later. The amplifier's noninverting output is fed back to its input through a capacitive divider formed by C_x and C_y, boosting the charge on C_x. The final value, determined by C_x, C_y, and amplifier gain, can be adjusted to equal the RF input voltage. As a result, when making absolute power measurements with Model 8754A, the RF-to-IF conversion efficiency varies less than 0.1 dB over the 5-30-MHz VTO range. In a ratio mode, the IF outputs of two samplers track typically within 0.02 dB.

Usable with External Sources

One of the advantages of the 8754A's sampling receiver is that it can be used with external sources. The receiver automatically locks to any suitable signal at the R input and tracks it while the signal sweeps. In this mode, the obtainable spectral purity and frequency accuracy is determined by the source used. For example, precision swept measurements of narrowband devices like crystal filters can be made by using a high-stability signal generator, such as the HP Model 8640A/B,[3] with a dc-coupled FM input that can be driven by the 8754A's sweep output. Or, synthesizers with highly accurate internal digital sweep may be used provided they supply an analog sweep output for control of the CRT horizontal axis and a blanking signal during frequency transients.

For proper phase lock, the receiver need only know the

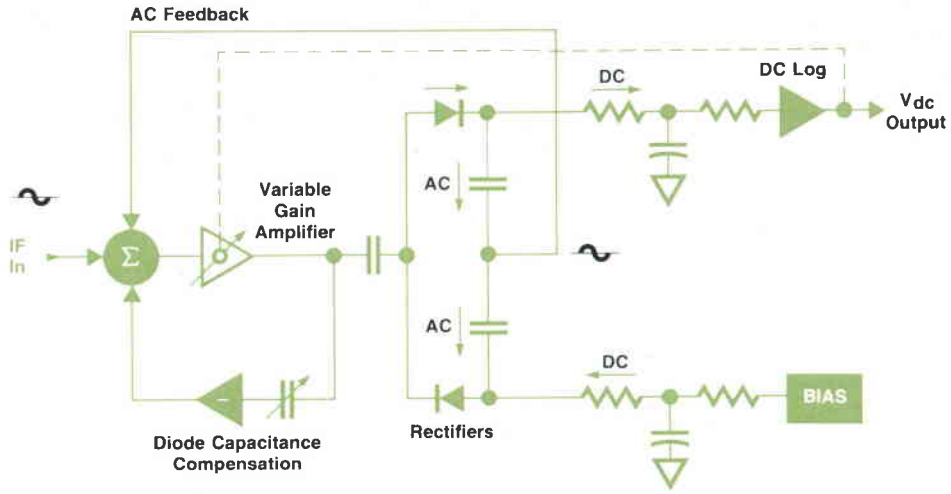


Fig. 12. *Magnitude detector has a full-wave rectifier within an ac feedback loop. Rectifier current is compared to the IF signal current at the input to the amplifier, which drives the diodes to make the two currents equal. Diode capacitance would cause an error in the diode current, limiting accuracy at low signal levels, but injection of an equal but opposite current into the summing node compensates for this. Also, the diodes' impedance changes with the input level. This affects the open-loop gain, giving rise to stability problems. Gain variations are reduced by a PIN-diode network within the amplifier that adjusts the gain according to the signal level.*

approximate frequency range of the external signal. For narrowband sweeps, tuning the LED frequency readout to the start frequency of the external source is sufficient. For sweeps wider than 1½ octaves, both the TUNING and SWEEP WIDTH controls are set on the 8754A to agree with the external source. For sweeps faster than 10 ms/div, the 8754A should supply the sweep voltage for the external source so the display transients at the relock points may be removed. For sweeps slower than 10 ms/div, as might be obtained from a sweeping synthesizer, there is no need to stop the sweep for relocking since the relocking occurs so quickly that it is barely visible on the display.

The sampling receiver is also capable of operating with input frequencies well above 1.3 GHz, though possibly with degraded performance. A modified version of the instrument, that will soon be available, will operate up to 2.6 GHz when using an external frequency doubler driven from the built-in source. Optional versions of the accessories (transmission/reflection test set, power splitters, etc.) will also be able to operate up to 2.6 GHz.

Magnitude Detectors

As was shown in Fig. 9, the A and B inputs time-share a detector. Channel switching is performed by an electronic switch that has 100-dB on/off isolation, assuring negligible IF cross-talk between channels.

The magnitude detectors are average-responding and use full-wave rectifiers in a feedback loop (Fig. 12). This assures a highly linear transfer function. The output current is processed through a logarithmic amplifier to derive a voltage proportional to the log of the IF level so the CRT's vertical scale can be in dB units. The basic circuitry was adapted from that used in the Model 8505A Network Analyzer.[4]

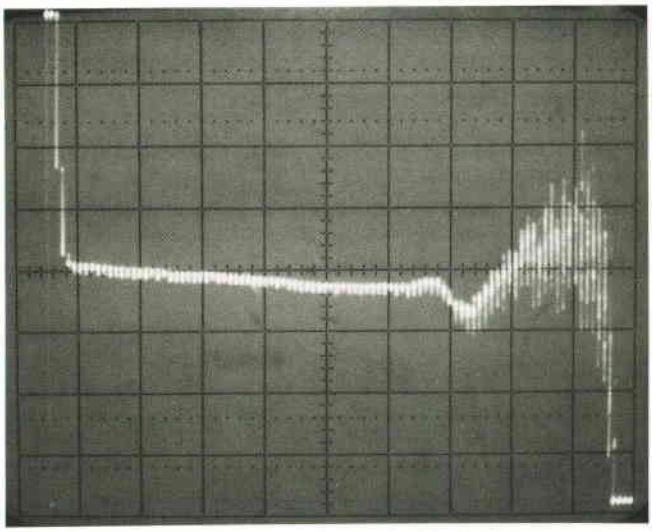


Fig. 13. *Oscilloscope display of magnitude detector error versus signal level over a range of +10 dBm (left) to −90 dBm (right). The error voltage is derived by comparing the detector output to a reference. This measurement, which shows the accuracy of the magnitude detectors, was made on a sweeping-attenuator test system developed for the 8754A production line. (Vertical scale: 0.25 dB/div.)*

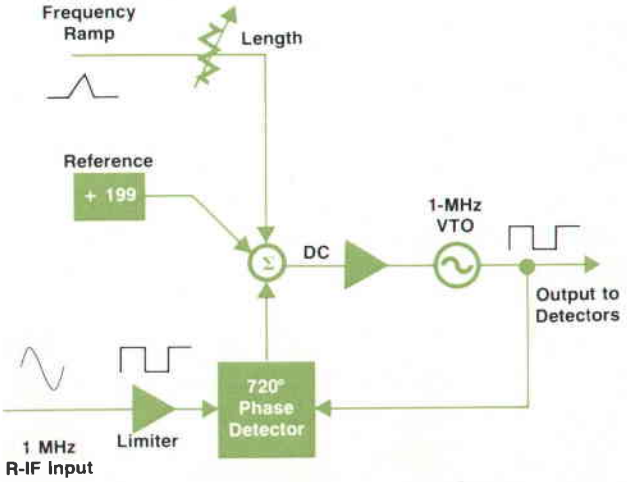


Fig. 14. *Phase shifter consists of a 1-MHz voltage-tuned oscillator (VTO) that is phase-locked to the R-channel signal with a phase offset.*

When the analyzer is displaying absolute power (dBm), the precision reference voltage discussed earlier is subtracted from the A/B channel output and the difference is amplified for presentation on the CRT. For ratio measurements, the R-channel voltage is subtracted from the A/B channel before the reference is subtracted. As shown by Fig. 13, this technique results in excellent dynamic accuracy. Devices can be measured with an uncertainty of only 0.01 dB/dB at levels within −10 to −40 dBm, and ±0.3 dB over a range of 0 to −50 dBm.

Phase Detector

An important design goal for any phase measuring instrument is retention of phase accuracy as the signal amplitude changes. In the 8754A, the two IF signals for the phase detector are processed through cascaded ECL line receivers to limit the amplitude excursions. The signals are thus subject to less than 2° phase shift over a 50-dB dynamic range.

The R-channel signal is processed through the phase-shifting circuit shown in Fig. 14. The signal is applied to a commercially available 720° phase detector where it is compared to the output of a 1-MHz voltage-tuned oscillator (VTO). The error voltage is summed with dc offset voltages and then used to control the VTO. The result is a 1-MHz signal that is phase-locked to the R-channel signal but offset in phase. The offsets come from the front-panel REFERENCE lever switch and the sweep tuning voltage. The front-panel switch enables a phase shift of up to ±199° to be introduced, and the attenuated sweep tuning voltage introduces a simulated time delay that can be adjusted to compensate for up to 16 cm of electrical length difference between the input cables.

Phase detection is accomplished with a conventional edge-triggered flip-flop.

The polar display is derived from a conventional resolver consisting of two analog multipliers in phase quadrature. The radius of the polar display, which is linearly proportional to the amplitude ratio, is obtained by processing the

ABRIDGED SPECIFICATIONS

HP Model 8754A Network Analyzer

Source

FREQUENCY RANGE: 4 MHz to 1300 MHz.

MARKERS:

SPACING: 1, 10, and 50 MHz.

ACCURACY: ±0.01%.

DIGITAL FREQUENCY READOUT: indicates frequency of variable tuning marker in linear FULL SWEEP mode, and start or center frequency in START and CENTER sweep modes.

RESOLUTION: 1 MHz.

ACCURACY: ±10 MHz (20° to 30°C). Readout is adjustable for calibration to internal crystal markers.

SWEEP WIDTH: selectable sweep widths from 1 to 1000 MHz in a 1, 2, 5 sequence, plus CW. Vernier allows continuous adjustment of sweep width within each range and calibration to internal crystal markers.

ACCURACY: typically ±2% (500 to 1000 MHz), typically ±5% (50 to 200 MHz), typically ±8% (1 to 20 MHz).

STABILITY:

TEMPERATURE: typically ±400 kHz/°C.

TIME: typically ±100 kHz/hour.

OUTPUT IMPEDANCE: 50Ω. Source match typically less than 1.4 SWR (>16 dB return loss).

POWER RANGE: calibrated 0 to +10 dBm. Uncalibrated to typically +13 dBm.

ACCURACY: ±0.8 dB at 50 MHz.

FLATNESS: ±0.5 dB.

SPECTRAL PURITY (+10 dBm RF output level):

SWEPT RESIDUAL FM (also applies to CW mode): ≤7 kHz rms (10-kHz bandwidth).

HARMONICS: −28 dBc (typically −35 dBc).

SPURIOUS: 4-500 MHz: −65 dBc (typically −75 dBc).

500-1300 MHz: −50 dBc (typically −60 dBc).

SWEEP TIME: typically 10 ms to 500 ms on FAST range, typically 1 s to 50 s on SLOW range.

TRIGGER MODES: AUTO (repetitive) and TRIG (single sweep triggered by front-panel button or rear-panel programming connector).

RF OUTPUT CONNECTOR: Type N female.

Receiver

FREQUENCY RANGE: 4 MHz to 1300 MHz.

INPUT CHANNELS: three inputs, R, A, and B. Two test inputs (A and B) with 80-dB dynamic range, and a reference input (R) with 40-dB dynamic range.

INPUT CONNECTORS: Type N female.

IMPEDANCE: 50Ω. Input port match ≥20 dB. Return loss (≤1.22 SWR).

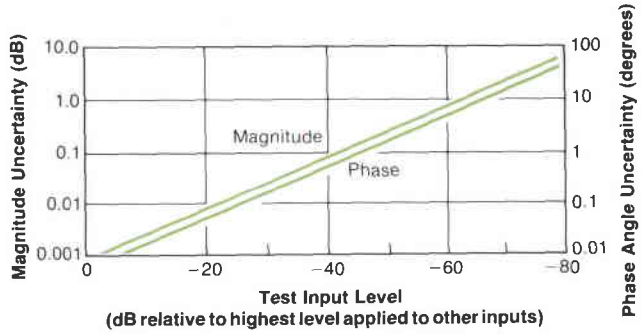
MAXIMUM INPUT LEVEL: 0 dBm.

NOISE LEVEL: < −80 dBm, A and B inputs.

MINIMUM R INPUT LEVEL: −40 dBm (≥−40 dBm required to operate R input phase-lock).

CROSSTALK BETWEEN CHANNELS: >83 dB.

ERROR LIMITS:



REFERENCE OFFSET:

RANGE: ±199 dB in 1-dB steps. Vernier provides typically ±80 dB of variable offset used for calibration in ratio measurements.

ACCURACY: included in Dynamic Accuracy above. Typically < ±0.1% of value.

DISPLAY RESOLUTION: 10, 2.5, 1, 0.25 dB/major division.

DISPLAY ACCURACY: ±2%, ±0.05 major division.

ERROR RESULTING FROM CHANGE IN HARMONIC NUMBER:

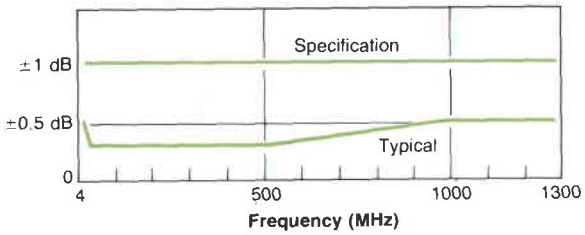
RATIO (A/R and B/R): typically ≤0.05 dB.

ABSOLUTE (A, B, AND R): typically ≤0.2 dB.

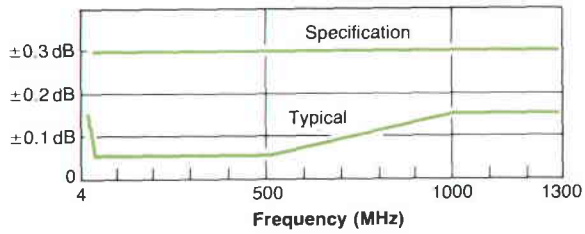
ABSOLUTE POWER (A, B, AND R): calibrated in dBm, typically < ±0.5 dBm with 0 dBm, 50 MHz input.

Magnitude

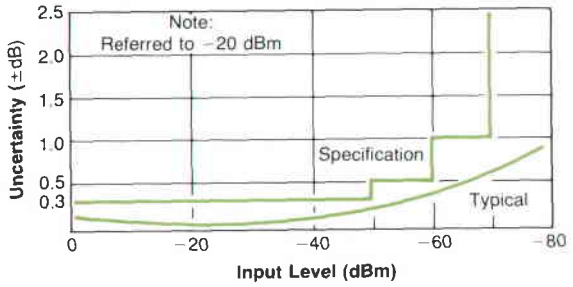
FREQUENCY RESPONSE (flatness): Absolute (A, B): ≤ ±1 dB.



RATIO (A/R, B/R): ≤ ±0.3 dB.

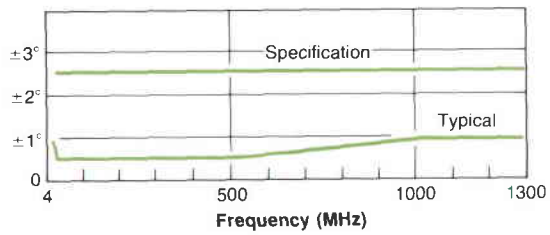


DYNAMIC ACCURACY (20-30°C):



Phase

FREQUENCY RESPONSE: ≤ ±2.5°.



RANGE: ±180°.

DYNAMIC ACCURACY:

±2° from 0 to −50 dBm.

±4° from −50 to −70 dBm.

REFERENCE OFFSET:

RANGE: ±199° in 1° steps. Vernier provides typically ±20° of variable offset used for phase calibration.

ACCURACY: ±1%.

DISPLAY RESOLUTION: 90, 45, 10, 2.5°/major division.

DISPLAY ACCURACY: ±2% ±0.05 division.

ELECTRICAL LENGTH ADJUSTMENT RANGE: typically 160 mm.

PHASE ERROR RESULTING FROM A CHANGE IN HARMONIC NUMBER: typically ≤0.5°.

Polar

See Magnitude and Phase specifications for frequency response, dynamic accuracy,

reference offset, and errors resulting from a change in harmonic number listed above.
DISPLAY ACCURACY: actual value is within 2.5 mm of displayed value.
ELECTRICAL LENGTH ADJUSTMENT RANGE: typically 160 mm, resulting in an 80-mm adjustment to the reference plane in a reflection measurement.

Display

MEASUREMENT FUNCTIONS: CRT displays either polar trace or two independent rectilinear traces.
CHANNEL 1: A,R magnitude absolute (dBm); A/R, B/R magnitude ratio (dB).
CHANNEL 2: B magnitude absolute (dBm); B/R magnitude ratio (dB); B/R phase (degrees).
POLAR: A/R magnitude ratio (dB) and phase (degrees).
REFERENCE POSITION: reference lines for Channel 1 and Channel 2 and polar center can be independently set to any position on the CRT for calibration. Display resolution expands about the reference position line.
VIDEO FILTER: typically 100 Hz (10 kHz without filter).
GRATICULE SIZE: rectilinear, 100 mm horizontal by 80 mm vertical; polar 80 mm in diameter. Both graticules internal to CRT.
SMITH CHART OVERLAYS: 2, 1, 0.2, and 0.1 full scale.
PHOSPHOR: P39.
CRT PHOTOGRAPHY: Electronic flash is required in the camera for graticule illumination. Ultraviolet (UV) illumination does not excite the P39 phosphor for graticule exposure.

Inputs/Outputs

SWEEP OUTPUT: −5 V to +5 V nominal, BNC female connector, used to frequency modulate (sweep) external generator.
EXTERNAL SWEEP INPUT: 0 to 10 V nominal. BNC female connector, used to sweep CRT display when receiver is used with external swept source, or to remotely program frequency of internal RF source from external digital-to-analog converter.
X-Y RECORDER/EXTERNAL CRT OUTPUT:
HORIZONTAL: 0.1 V/div (0 to 1 V).
VERTICAL: 0.1 V/div (±0.4 V full scale).
PENLIFT/BLANKING: +5 V blanking and penlift; −5 V intensifies crystal markers.
EXTERNAL MARKER INPUT: typically −13 dBm RF signal into EXTERNAL MARKER Input produces amplitude (rectilinear) or intensity (polar) marker on trace at frequency of RF signal. BNC female connector, 50Ω.
MAGNITUDE/PHASE OUTPUT: −10 mV/degree and −100 mV/dB at BNC female connector. Multiplexed by TTL level or contact closure at pin of programming connector for use with external digital voltmeter.
ACCURACY: see magnitude dynamic accuracy specifications
PHASE SCALE ERROR: ±1.5% (≤170°); ±2% (±180°).
PROBE POWER: +15 Vdc and −12.6 Vdc, for use with HP 10855A Preamp or HP 1121A AC Probe. Two probe power jacks are provided.
STORAGE-NORMALIZER INTERFACES: directly compatible with both the HP 8750A Storage-Normalizer and the HP 8501A Storage-Normalizer. All 8501A features except CRT labels and graphics are available when 8501A is used in conjunction with 8754A.
PROGRAMMING CONNECTOR:
FUNCTION: 25-pin Amphenol connector (with mating connector) includes magnitude/phase and sweep outputs and inputs described above and measurement mode selection by TTL levels or contact closures.

General

OPERATING TEMPERATURE: 0° to 55°C except where noted.
SAFETY: conforms to requirements of IEC 348.
POWER: 100, 120, 220 and 240 V, +5% −10%. 48 to 66 Hz, 200 VA max.
SIZE: 133 mm H × 425 mm W × 505 mm D (5¼ × 16-3/4 × 19⅞ in).
WEIGHT: 17.7 kg (39 lb).
PRICE IN U.S.A.: $11,500.
MANUFACTURING DIVISION: SANTA ROSA DIVISION
1400 Fountain Grove Parkway
Santa Rosa, California 95404 U.S.A.

logarithmic outputs of the magnitude detectors through an exponential amplifier.

Semi-automated System Capability

Although the 8754A is intended primarily for use as a manually operated bench instrument, provisions were made for its use in semiautomatic systems. The RF source can be swept by an externally supplied voltage over the frequency range selected on the front panel. This voltage could be provided by a digital-to-analog converter. A rear-panel output proportional to log magnitude ratio or phase angle, as selected by a TTL programming voltage supplied to a rear-panel connector, is available. This output could be applied to a digital voltmeter (outputs for an X-Y recorder are also provided). Techniques for configuring the 8754A for operation on the HP Interface Bus* are described in HP Application Note No. 294.

Acknowledgements

Fred Rawson designed the power supplies, sweep circuitry, display circuits, marker generator, and polar/phase detectors. Mike Sohigian was responsible for the source and amplifier/detector microcircuits. Fred Woodhull designed the magnitude detector. Phil Luque did the initial receiver investigation before transferring to HP's Boise Division. Jim Jones and Steve Sparks developed the phase-lock system. Dick Barg did the product design and Chuck Compton provided production engineering support. Thanks are also due Bill Kabage, Russ Johnson, Joe Williams, Sam Zuck, Jim Stead, Roy Church, and Bill Simmons, and special thanks to Doug Rytting, lab section manager, who inspired the initial concept and provided support along the way.

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*Hewlett-Packard's implementation of ANSI/IEEE 488-1978

James R. Zellers

A native of Los Angeles, California, Jim Zellers earned a BSEE degree from the University of California at Berkeley in 1966, then designed crystal oscillators for a year, returned to school to obtain an MSEE degree (University of Michigan, 1968), and shortly thereafter joined Hewlett-Packard in Palo Alto. At HP he worked initially on cesium-beam frequency standards, and then became involved in automatic network analyzers, microwave signal generators and sweepers before taking on project leadership of the 8754A Network Analyzer. Now living in Santa Rosa, California, with his wife and two young children (ages 3 and 5), Jim enjoys tent camping with his family, photography, woodworking, music, and hi-fi.

Expanding Logic Analyzer Capabilities by Means of the HP-IB

Augmenting the power of a logic state/timing analyzer with a desktop computer gives automated testing capability along with display in user-definable assembly language.

by Robert G. Wickliff, Jr. and Richard A. Nygaard, Jr.

BY PROVIDING A MEANS of monitoring the sequential states of digital processor systems, logic state analyzers, first introduced in 1973,[1] quickly established themselves as indispensable tools for the design, development, and servicing of digital systems.

Later versions of the logic state analyzer made it easier to monitor complex state flow involving program branching, looping, and subroutines.[2] Logic timing analysis has also been incorporated so that glitches and other transients that derail correct state flow can be located.[3]

Now, by equipping two of HP's logic analyzers, Models 1610A/B[2] (Fig. 1) and 1615A[3] (Fig. 2), to operate with the HP interface bus,* another step forward in capability has been added. The ability to communicate over the HP-IB enables the analyzer to interact with a computer, making programmed control of the analyzer possible for both laboratory and production-line applications. For example, state-flow data captured by either of these analyzers from a microprocessor system can be converted by the computer to the mnemonics of that particular microprocessor, regardless of what type it is, and then passed back to the analyzer for display. With the conversion to mnemonics, interpretation of data becomes much easier than it would be if it were left in binary. Also, statistical analyses can be performed on the data, such as the percentage of time spent in a given address range, the number of read errors encountered during mass storage access, and the number of calls to a subroutine.

"Babysitting" an intermittent problem is another task that is greatly simplified by analyzer-computer interaction. Measurements may be set up for repetition under program control. Twenty-four hours a day, the computer can compare automatically acquired measurement results with stored data and accumulate information about occasional errors. No one has to stay there to note the fault, and restart the measurement.

Easy documentation is another advantage. Any part or all of an analyzer's memory can be printed out by the computer for inclusion in lab notebooks. Accurate diagrams of signal

*Hewlett-Packard's implementation of ANSI/IEEE 488-1978.

Fig. 1. *Model 1610A/B Logic State Analyzer traces the flow of simultaneous digital events in as many as 32 bus lines in digital systems at clock rates up to 10 MHz. Its selective triggering capabilities enable it to restrict data capture to specific loops or branches in complex programs. Keyboard control and an interactive display that uses menus enable rapid set up of complex measurement parameters. The Model 1610B shown here can have data strobed in by three different clocks.*

Fig. 2. *Model 1615A Logic Analyzer can function as a 24-bit state analyzer, an 8-bit timing analyzer with glitch triggering capability, or as a combination 16-bit state and 8-bit timing analyzer that captures time and state activity simultaneously. Cross triggering between timing and state modes enables study of the interaction between timing problems and particular states, especially useful where the system under test has both synchronous and asynchronous elements.*

timing as well as any glitches that are present (when using the Model 1615A) can be plotted for before-after comparisons pertaining to a design change.

Automated Measurements

Faster prototype development can result from use of the analyzer-computer combination. Complex measurement set-ups and the expected results are easily stored within the computer for later use. For example, operation of a fairly simple module in the breadboard stage recently required nearly half a day for verification. Most of this time was spent in manually setting up trace conditions on the logic analyzer and checking the captured data. A simple program incorporating the setup conditions and data was then written. As a result, when the prototype boards came back from the shop, the analyzer-computer system needed only five minutes to determine that the prototypes functioned just like the breadboard.

Production-line testing is an obvious application of the analyzer-computer combination. Tests developed in the lab during the design phase to verify performance, such as in the preceding example, can be used in production. This has an additional advantage in that production tests can be traced back to the design engineer and when special problems arise, the design engineer won't have to spend extra time understanding unfamiliar production test equipment and procedures.

Also on the production line, troubleshooting can be simplified by the use of interactive test selection, employing the analyzer's CRT to present options and suggested procedures to the test technician.

Servicing procedures in the field can also be improved by use of an analyzer equipped with the HP-IB option. An HP-IB-to-RS-232C(V.24) interface that would enable communications between a logic analyzer in the field and a computer at a central site would make the expertise of a service engineer at the central site available to a technician in the field. The analyzer in the field can display messages sent from the central site and, if the analyzer is a 1610A/B, the analyzer's keyboard can be used to respond. In addition, the remote unit can be effectively slaved to another unit at the central site, enabling the service engineer to run traces and see the results without leaving the central site.

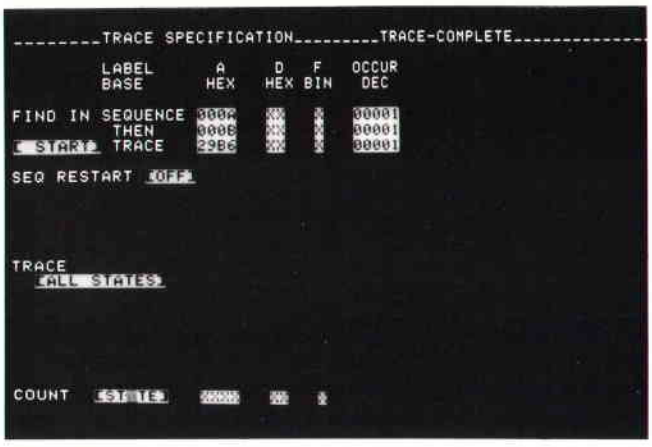

Fig. 3. *Menus display fields (highlighted by inverse video) that may be changed by the keyboard in setting up instrument controls. The menu shown here tells the analyzer it must first find state 000A and then 000B in that order before allowing state 29B6 to start data capture.*

Straightforward Programming

In the design of the HP-IB interfaces for the Models 1610A/B and 1615A, programming convenience was a major consideration. Experience has shown that two-character mnemonics provide sufficient program readability along with conciseness. With instruments, the mnemonics usually are associated with specific front-panel controls and are generally printed right on the front panel next to the associated control. The Models 1610A/B and 1615A, however, are each controlled by a simplified keyboard and use a CRT to display the control settings (Fig. 3). There is no direct association between the front-panel controls and instrument functions. Therefore, the mnemonics that were selected for the HP-IB interfaces are associated with specific data fields within the menus that the instrument displays.

Each mnemonic was chosen to provide ready association with the function it controls. For example, a trace point specification begins with the mnemonic TP and a sequence term begins with SQ. Additional information is supplied with an operand and/or parameters. The operand in the trace-point command specifies whether the designated trigger state is the start, center, or end point of the trace. Thus, TP1,0500 starts the trace on the occurrence of state 0500 in the logic-state flow while TP3,0500 ends the trace on the same state.

Multiple parameters within a command are separated by commas. In many cases, the parameters are loaded directly into the data fields in the displayed menus. For example, the string LSAAAAAAAA,AAAAAAAA,CCCCCCCC would set up the label-select field as shown in Fig. 4.

Commands that require an operand or parameter(s) also require an explicit terminator to signify the end of a command and initiate its execution. Because a terminator is required, hexadecimal characters may be used for operands and parameters; no confusion can occur with the mnemonic of a following command because it cannot be executed until the current command has been terminated.

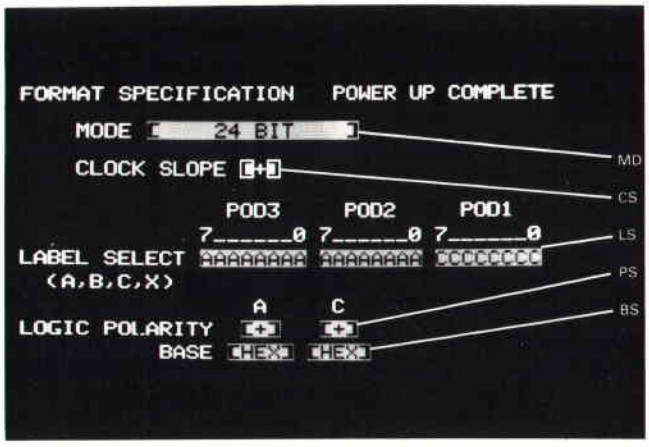

Fig. 4. *Two-letter mnemonic commands sent over the HP-IB, shown in column at right, are alphabetically related to specific data fields within the menus.*

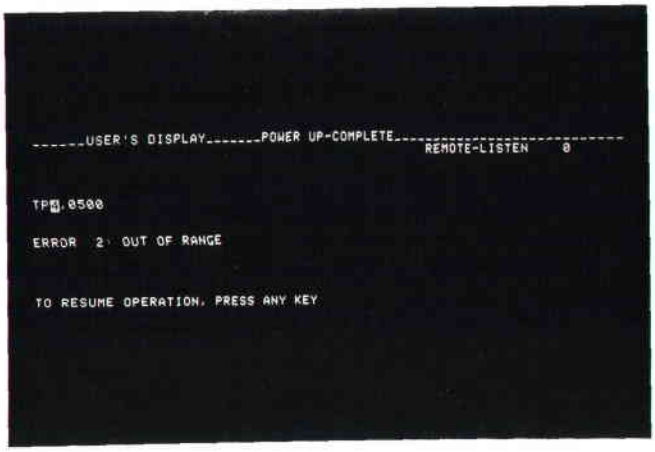

Fig. 5. *When an illegal command is sent over the HP-IB to Model 1610A/B, the analyzer displays an error message. In the one shown here, number 3 is the highest value that can follow the mnemonic TP (trace point).*

Line feeds and carriage returns are ignored in most cases since they are usually difficult to suppress. The exceptions are commands containing data, in which a carriage return would be valid data, or text strings in which a line feed would be a valid terminator.

When the logic analyzer receives a command over the HP-IB, the menu to which it refers is displayed automatically and the referenced field is updated. By watching the display, a programmer gets immediate feedback about the effects of programmed commands. Programming these analyzers over the HP-IB is therefore very much like operating them from the front panel.

If the Model 1615A detects an error in a programmed command, the display flashes ERROR-INVALID ENTRY just as it would under local control. If Model 1610A/B detects an error in a command, such as an out-of-range operand, it displays the entire command, with the erroneous operand highlighted in inverse video, along with an error number and description. Operation may be resumed by pressing a key. Alternatively, Model 1610A/B can be programmed to generate a service request when an error is detected. The error number can then be read and program execution resumed by reading a status byte over the HP-IB (Fig. 5).

Fast Programmed Setup

The HP-IB interfaces also provide a "learn" mode for the analyzers. Sending the learn command causes either analyzer to output a packed binary string containing the status of all analyzer control functions preceded by an identifier. When the string is returned to the analyzer at a later time, the identifier sets the analyzer to receive the packed setup information and the analyzer control functions are set as they were when the string was originally sent. Thus, the analyzer may be set up manually and the controller, usually a desktop computer, can read and store the complete setup. Consequently, programs need only a few commands to control the analyzer completely. Tests may be performed on a device that is known to be good and the test results saved along with the setup information. Tests on other units may then be performed by first sending the learn string and then comparing the new test results to the stored data. Furthermore, the test setup and test results may be stored in arrays and do not need to be written as part of a program. A single control program that calls up the stored arrays may then be used for many different tests, thus keeping software costs at a minimum.

The HP-IB interfaces also provide a TALK-ONLY mode, selected by a rear-panel switch. In this mode, the analyzers respond normally to their keyboards but when the PRINT key is pressed (STOP/PRINT on the 1615A), if a trace is not in process the analyzer will output the current display in ASCII over the HP-IB. This enables hard-copy output without requiring a controller (Model 1610A/B also has an output for driving an HP Model 9866A/B thermal line printer directly, a standard feature).

The HP-IB interface for Model 1615A can also output its timing diagram display using the HP graphics language (HP-GL)[4] to generate plots and labels for the plots on any of the HP plotters that interface to the HP-IB (Fig. 6). The other

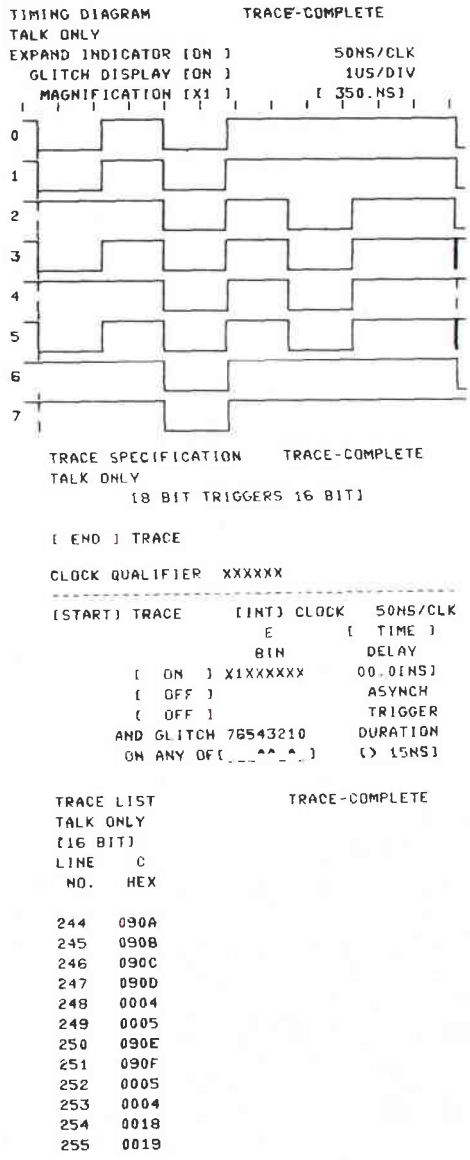

Fig. 6. *Timing plots and labels can be sent from Model 1615A over the HP-IB to a digital plotter.*

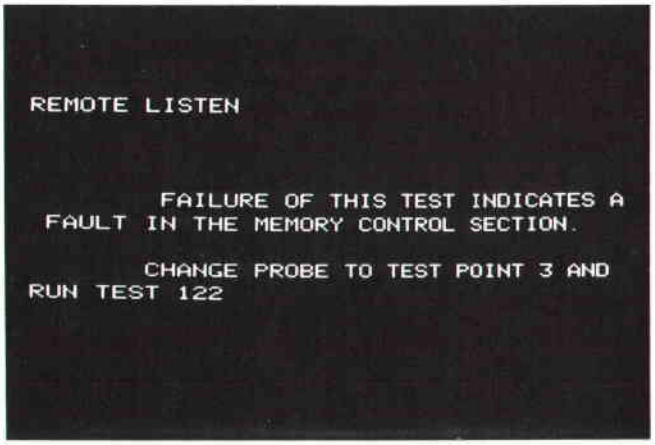

Fig. 7. *Automatic test programs for controlling a logic analyzer over the HP-IB can include messages that are displayed on the analyzer's CRT for the test technician.*

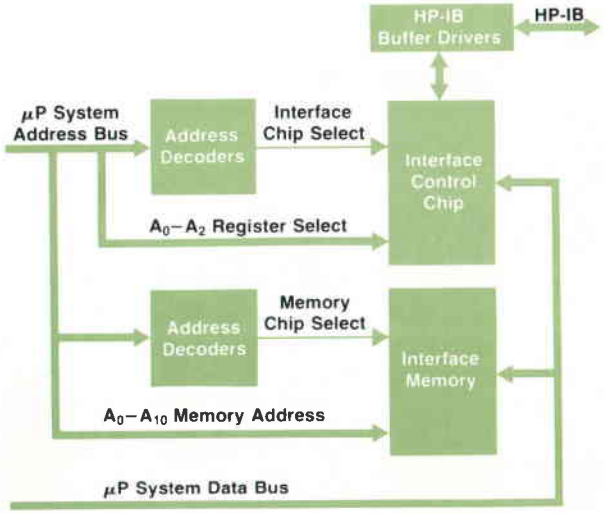

Fig. 8. *Generalized block diagram of the interface between logic analyzer and the HP-IB.*

displays (menus and data lists) are output in 7-bit ASCII and require a separate printer (except for the HP Model 7245A Plotter/Printer that can provide both types of copy[5]). These same outputs are also available under program control through the print (PR) command.

The controller may also write messages directly on the analyzer display (Fig. 7). The display characters (DC) command can access all but the top two lines on the display, which are reserved for status and error messages including HP-IB status information. Three parameters following the DC command specify normal, inverse, or blinking characters, and the line and column where the message is to start. ASCII-coded text can then follow these parameters.

Hardware Approach

The HP-IB interfaces were designed so as to impact the existing logic analyzer designs as little as possible. Consequently, each interface consists of a single printed-circuit board and associated cabling. It is thus possible to retrofit the interfaces to analyzers already in the field.

The interfaces were also designed so as not to interfere with the normal operation of the host analyzer. Each interface therefore has its own firmware package.

A block diagram is shown in Fig. 8. Asynchronous control logic for the HP-IB functions is implemented by an interface control IC chip (MC 68488 in the 1615A, HP's PHI chip[6] in the 1610A/B). The analyzer's microprocessor controls the interface chip by writing to a bank of registers internal to the chip. All communications between the HP-IB and the microprocessor flow through these internal registers.

To enable either analyzer's operating system to detect whether or not the HP-IB interface is installed, during the normal keyboard scan routine the analyzer addresses the first byte in the HP-IB ROM. The analyzer's data bus has pull-up resistors so if the data lines are pulled low in response to the address, the analyzer's operating system knows that the interface is installed. The operating system will execute a jump to the HP-IB area only if the interface is present. Locating the interface check ahead of the keyboard scan routine allows keyboard operation to be inhibited until the interface firmware passes control back to the analyzer's operating system.

The interface code is implemented using formatters (subroutines) and table descriptions of each command. Each formatter handles several functions that are basically similar. Hence, only five formatters are required for the 1615A, and nine for the 1610A/B.

A look-up table links each mnemonic to a table containing the address of the proper formatter and instruction bytes for that formatter. The instruction bytes point to the menu and field prescribed and any restrictions on parameter values. The code required for a given command thus consists of only a few table entries rather than a long subroutine.

The operating system in the Model 1610A/B was modified to allow interaction between the 1610A/B's operating system and the HP-IB interface firmware. To allow the firmware modules to interact correctly, the addresses of all global routines are included in tables within the ROM space of each. These tables start at a known location within each module and include jump instructions that transfer a subroutine call to the correct address within the module. The calling location thus is unaware of the ultimate destination. The practical advantage of using tables rather than directly calling the routines arises in the event that software modifications and relocations are required. Only the jump address needs to be modified to accommodate the change. Many ROMs that otherwise would have to be replaced may thus be left unchanged.

Acknowledgments

Many people participated in the design of these interfaces. Don Corson helped in the functional definitions. Justin Morrill, project leader for the 1610A/B, provided guidance and a discerning ear to new ideas and John Hansen helped with the hardware design of the 1610A/B HP-IB interface. Harry Short did the mechanical design for the 1615A HP-IB interface, and project leader John Scharrer provided design help and encouragement.

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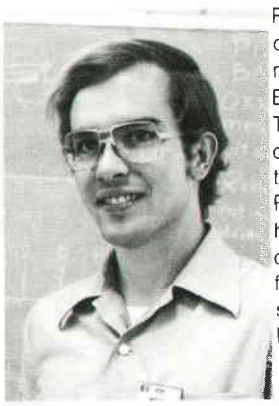


Richard A. Nygaard, Jr.

Rick Nygaard came to work for the Colorado Springs Division of HP immediately after he completed his Bachelor's degree in EE at Georgia Tech in 1977. His first project at HP was contributing firmware modifications for the 1610B Logic State Analyzer. Then Rick was assigned to preparing the hardware and firmware for the HP-IB option for the 1610. Rick bicycles to and from work, and rides his bike for pleasure, too. He also enjoys woodworking, hiking and camping.

Robert G. Wickliff, Jr.

Bob Wickliff joined HP in 1974, initially working on CRT design, then the Logic Analyzers, and most recently the hardware and firmware for the 1615A's HP-IB interface. A native of Columbus, Ohio, Bob obtained BSEE (1969) and MSEE (1970) degrees from Ohio State University and worked on electronic countermeasures as a graduate research associate before joining HP. In off hours, Bob spends time on photography. When time permits, Bob and his wife like to fly to far away places like Alaska and go camping there.

ABBREVIATED SPECIFICATIONS

HP Model 1610A/B Logic State Analyzer

CLOCK AND DATA INPUTS
- REPETITION RATE: to 10 MHz.
- INPUT THRESHOLD: TTL, fixed at approximately +1.5 V; variable, ±10 Vdc.
- MINIMUM INPUT
  - SWING: 0.6 V.
  - CLOCK PULSE WIDTH: 20 ns at threshold level.
  - DATA SETUP TIME: 20 ns.
  - HOLD TIME: 0 ns.
- MULTIPHASE CLOCKS (1610B only): Data is strobed in on either or both edges of up to three qualified clocks. Used separately, clock 1 strobes in 16 bits, clock 2 strobes in 8 bits, and clock 3 strobes in 8 bits. Clocks may be logically ORed.

TRIGGER AND MEASUREMENT ENABLE OUTPUTS
- TRIGGER OUTPUT (rear panel): 50 ns ±10 ns positive TTL level trigger pulse is generated each time trace position is recognized.
- MEASUREMENT ENABLE OUTPUT (rear panel): Positive TTL level measurement enable output goes high and remains high when 1610A is looking for trace position and goes low when trace position is recognized or if STOP key is pressed.

MEMORY DEPTH: 64 data transactions; 20 transactions are displayed on screen. Roll keys permit viewing all 64 data transactions.

TIME INTERVAL: Resolution, 100 ns; accuracy, 0.01%; maximum time, 429.4 seconds.

EVENTS COUNT: 0 to $2^{32}-1$ events.

DIMENSIONS: 230 mm H × 425 mm W × 752 mm D (9.063 × 16.75 × 29.625 in).

WEIGHT: 1610A, 26.5 kg (58.5 lb). 1610B, 23.8 kg (52.5 lb).

ACCESSORIES SUPPLIED: four 10248A data probes, one 10247A clock probe.

OPTION 003: Adapts analyzer for use in systems linked by the HP Interface Bus (HP-IB). It receives commands via the HP-IB that stimulate front-panel keyboard entries and cause the analyzer to assume a measurement configuration, execute traces, and configure itself to transmit results to other instruments on the HP-IB.

PRICES IN U.S.A.: 1610A, $11,000; 1610B, $12,500; Opt 003, $800 (1610A) or $700 (1610B).*

*When included with initial order. Model 10494A Field Kit ($1200) retrofits 1610A's with serial number prefixes below 01610-1813, Model 10495A Field Kit ($900) retrofits 1610A's with serial number prefixes above 01610-1821, and Model 10496A Field Kit ($800) retrofits all 1610B's.

HP Model 1615A Logic Analyzer

CLOCK QUALIFIER AND DATA INPUTS
- REPETITION RATE: to 20 MHz.
- INPUT THRESHOLD: TTL, fixed at approximately +1.4 V; variable ±10 Vdc.
- MINIMUM INPUT
  - SWING: .6 V.
  - CLOCK PULSE WIDTH: 20 ns at threshold level.
  - SETUP TIME: 20 ns.
  - HOLD TIME: 0 ns.

SYNCHRONOUS OPERATION
- TRIGGER DELAY: to 999,999 clocks.
- TRIGGER OCCURRENCE: to 999,999.

ASYNCHRONOUS OPERATION
- SAMPLE RATE: 2 Hz to 20 MHz.
- MINIMUM DETECTABLE GLITCH: 5 ns with 30% peak overdrive or 250 mV, whichever is greater.
- GLITCH TRIGGER: on any selected channel(s), if glitch is captured, glitch is ANDed with asynchronous pattern trigger.
- EXTERNAL TRIGGER PULSE WIDTH: 5 ns minimum with 30% peak overdrive or 250 mV, whichever is greater.
- PATTERN TRIGGER: any 8-bit pattern. Trigger duration required is selectable 15, 50, 100, 200, 500, 1000, or 2000 ns ±15 ns or 15%, whichever is greater.
- DELAY TIME: to 1, 048, 575 × sample period.

TRIGGER OUTPUTS (rear panel)
- 16/24 BIT TRIGGER OUTPUT
  - LEVEL: high, ≥2 V into 50Ω; low, ≤0.4 V into 50Ω.
- 16/24 BIT TRACE POINT OUTPUT
  - LEVEL: high, ≥2 V into 50Ω; low, ≤0.4 V into 50Ω.
  - PULSE DURATION: starts at beginning of trace and ends at trigger point (pattern trigger plus delay).
- 8-BIT PATTERN OUTPUT
  - LEVEL: high, ≥2 V into 50Ω; low ≤0.4 V into 50Ω.
  - PULSE DURATION: pattern duration minus asynchronous trigger duration width.

MEMORY DEPTH: 256 data transactions (in timing display mode, 249 samples are displayed).

POWER: 100, 120, 220, 240 Vac, −10% to +5%; 48 to 66 Hz; 230 VA max.

DIMENSIONS: 189 mm H × 426 mm W × 664 mm D (7.438 × 16.75 × 26.125 in).

WEIGHT: 19.1 kg (42 lb).

ACCESSORIES SUPPLIED: three 8-bit Model 10248B data probes and one Model 10248B opt 001 clock probe with probe leads and tips (three for data and one for clock, qualifiers, and external trigger).

OPT 001: Adapts analyzer for use in systems linked by the HP Interface Bus (HP-IB). It receives commands via the HP-IB that stimulate front-panel keyboard entries and cause the analyzer to assume a measurement configuration, execute traces, and configure itself to transmit results to other instruments on the HP-IB.

PRICES IN U.S.A.: 1615A, $6800; Opt 001, $400; 10069A HP-IB Field Kit, $400.

MANUFACTURING DIVISION: COLORADO SPRINGS DIVISION
1900 Garden of the Gods Road
Colorado Springs, Colorado 80901 U.S.A.

A Serial Data Analyzer for Locating Faults in Decentralized Digital Systems

Interfaced to the RS-232C (V.24) data communications bus, this instrument can monitor data traffic on the bus to help identify an operational problem. It can then assume an active role and substitute for the CPU, a terminal, a peripheral, or a modem to help isolate the problem.

by Robert E. Erdmann, Jr.

THE TROUBLESHOOTING OF computer systems is becoming increasingly difficult as more and more use is made of serial data links to tie a system together. For example, if a terminal at a remote location cannot communicate with the central processing unit (CPU), does the fault lie in the terminal, in the CPU, or in the serial data link? And if the data link involves a phone line and modems, is the fault in one of the modems or the phone link itself?

The Model 1640A Serial Data Analyzer (Fig. 1) was developed to track down faults in multi-unit systems of this nature. This instrument has an RS-232C (V.24) connector that allows it to be connected into a system wherever the data has been put into serial form for transmission over an RS-232C-compatible link. Connected into a system, Model 1640A can function like a logic state analyzer to capture and store data being transmitted on the RS-232C link beginning or ending with the occurrence of a specified trigger sequence or other trigger (trapping) event. It may thus display selected blocks of activity on the link, showing both the received and transmitted data to help identify the source of a problem. In this monitor mode, it bridges the RS-232C bus and has no influence on system operation. It is essentially transparent to the units communicating on the link.

In its simulate mode, Model 1640A can substitute for a CPU, or modem peripheral to help isolate a fault. If a terminal is suspected, the terminal can be disconnected from the system and connected to the 1640A which then "talks" to

Fig. 1. *Model 1640A Serial Data Analyzer is a portable logic analyzer tailored for the troubleshooting and analysis of systems tied together by serial data communications buses. Its capability for both monitoring and simulation enables it to analyze a whole spectrum of problems associated with malfunctioning systems that use communications buses.*

the terminal using a language and handshaking protocol that the terminal can respond to. If it turns out the terminal is not at fault, the 1640A may be connected to the system in place of the terminal, and it can interact with the system as the terminal would by generating and responding to specific messages. Similarly, it may be used at the CPU end to simulate the transmission link in tests of the CPU, or exercise the transmission link in place of the CPU.

Appropriate messages for the simulation tests may be entered into the 1640A by way of the 1640A's keyboard, or copies of actual network protocol captured in the 1640A's monitor memory may be entered automatically into its transmit memory and edited for subsequent use. Complicated messages that are used frequently may be stored in PROMs and plugged into the 1640A for quick recall when needed.

Response to Timing Errors

Among the several fault-finding capabilities provided in this instrument is a timing capability. The 1640A may be set to time the interval between a handshake signal and the response to it, or the time between the start of a block of transmit data and the start of the subsequent block of receive data.

Timing violations can be used as triggers to initiate the capture and display of characters preceding and following the timing violation to assist in tracking down the causes of faults.

Other triggering modes that are available include triggering on the occurrence of a data or parity error, triggering on a specified character (up to 8 bits), and triggering only when a specified character contains an error.

Coding Flexibility

The 1640A can work with various code sets. ASCII, EBCDIC, and hexadecimal are standard and the capability for working with other codes is available. The instrument can operate synchronously or asynchronously at rates up to 19.2 kb/s with error checking on odd or even parity or without parity. Cyclic redundancy error checking (CRC-16, LRC, CRC-CCITT) is available as an option, as is full SDLC/HDLC (synchronous data link control/high level data link control) capability. In the synchronous mode, there is a choice of character framing on either one or two synchronizing characters that are user definable, as is the resynchronizing capability.

Menu Control

Because of the large number of functions that this instrument can perform—and the permutations and interactions of functions—a key-per-function arrangement of the control panel would have been overly complicated. Instead, a "menu" approach with directive displays and a simplified keyboard is used.

The top line of the display identifies the menu selected by keys in the DISPLAY group (see Fig. 1). The second line contains any messages for the user concerning incorrect operation. On the next lines, the blocks (fields) in inverse video (black on white) indicate where entries are to be made from the ENTRY section of the keyboard. Annotation adjacent to the inverse-video blocks explains the meaning of each block (Fig. 2).

The user inputs data by first using the CURSOR keys, which move a blinking cursor to the desired entry field. Brackets in an entry field indicate that inputs to this field are controlled by the FIELD SELECT key. Pressing this key causes the entry field identified by the cursor to cycle through its allowable choices. Data for other fields is entered through the hexadecimal keypad.

The FORMAT menu is used to configure the 1640A for compatibility with the incoming or outgoing serial data stream. This includes code set, baud rate, sync or async operation, specification of the sync character, resync specification, and error checking/generation capabilities.

The MODE menu is used to tell the 1640A what to do. This includes monitor or simulate, half- or full-duplex operation, transmit or receive first, trigger (trapping) source, and the trigger sequence. It also includes the reply-on-character sequence (in the simulate mode, tells the 1640A the character sequence that, when received, should cause the 1640A to transmit back a user-defined response), run mode (trigger starts display, trigger ends display, count triggers, etc.), and what data should be suppressed to save memory space, such as syncs, nulls, idles, and all but the trigger and N characters following.

The TX ENTRY menu allows the user to define what is to be transmitted in the simulate mode. The message may be entered through the hexadecimal keypad or automatically copied from data previously received and stored in the monitor memory. The copied data may be edited and may be broken up into as many as eleven blocks if so desired.

The LIST menu shows what was captured and stored in the monitor memory. TX and RX data may be viewed separately or both can be viewed together, interleaved according to the relative time of occurrence of each character. In this case, the TX data is displayed in normal video and the RX data in inverse video (Fig. 3). Only about one-fourth of the

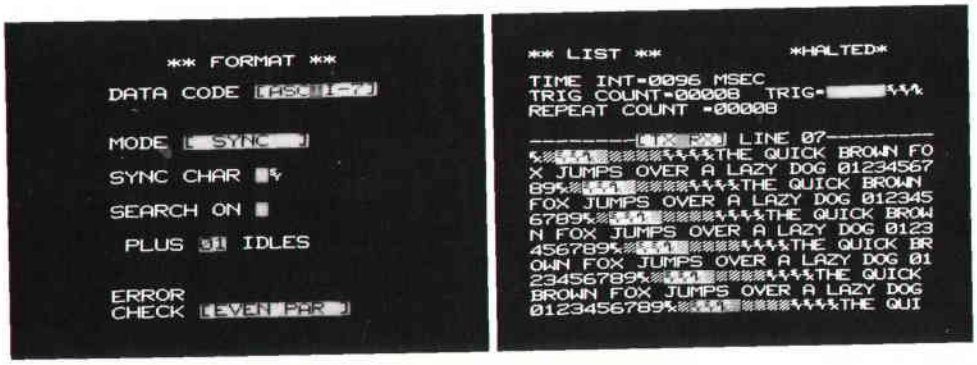


Fig. 2. *(Left) Typical menu shows the selections to be made, in this case the format for configuring the instrument to match the format of the data in the RS-232C bus. The blinking cursor is positioned here in the* DATA CODE *field.* **Fig. 3.** *(Right) In the* LIST *mode, the contents of the data-acquisition memory are displayed with* RX *data (inverse video) interleaved with* TX *data (normal video).*

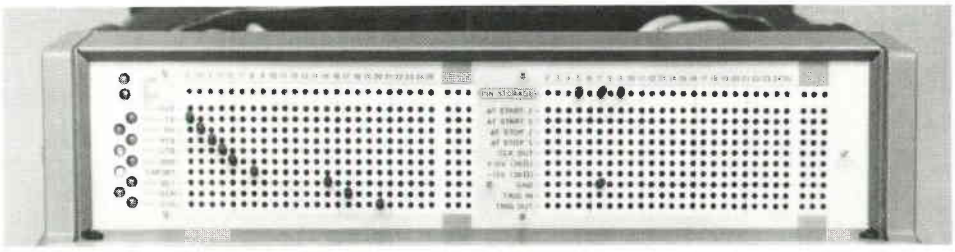


Fig. 4. *The pin matrix enables the connection of any lead in the RS-232C bus to any input or output of the 1640A by insertion of a metal pin where the leads cross. The pin configuration shown here is the one most often used.*

memory can be displayed at one time but the rest can be brought on display by using the up-down CURSOR keys to scroll the data past the display.

External Control

With the optional HP-IB* interface installed, the 1640A can be operated by an external controller. Each of the entry fields on the menus can be programmed individually through the HP-IB or the 1640A can be completely programmed all at once by sending it a "learn" string from the controller.

HP-IB control not only permits remote operation of the 1640A, but it also enables more sophisticated testing. Data acquired by the 1640A can be transferred over the HP-IB to a controller for mass storage, for statistical analyses, or for examination to find particular sequences. The controller can make decisions on what message to transmit based on the messages received, or repetitively alter messages to check for pattern sensitivity.

An additional capability of the HP-IB interface is that it allows up to ten user-defined instrument setups to be stored in PROM in the instrument and then selected and loaded with a rear-panel switch. Often-used setups may thereafter be recalled simply by pressing a single key.

*Hewlett-Packard's implementation of ANSI/IEEE 488/1978

Pin-Matrix Connector

Because of the variety of uses for the Model 1640A, a pin-matrix interface is included with the instrument for making the connections to the RS-232C bus. This matrix (Fig. 4) allows any lead on the RS-232C bus to be connected to the appropriate input or output of the 1640A just by inserting a metal pin where the particular RS-232C lead crosses the 1640A input or output. For example, for asynchronous monitoring, pin 2 (transmitted data) of the RS-232C bus is connected to the TX output of the 1640A, pin 3 (received data) is connected to the RX input, and pin 7 (common return) to ground. All others are left open.

The diagram of Fig. 5 illustrates the pin-matrix organization. LED indicators show the status of any of the 1640A's inputs or outputs. Besides the normal RS-232C connections to the 1640A, inputs are provided that allow any line in the RS-232C bus to start or stop a time-interval measurement or to supply a trigger for data acquisition. To simplify interconnections for often-made measurements, Mylar overlays are provided. Some of these have prepunched holes where pin connections are to be made, and others are left blank so

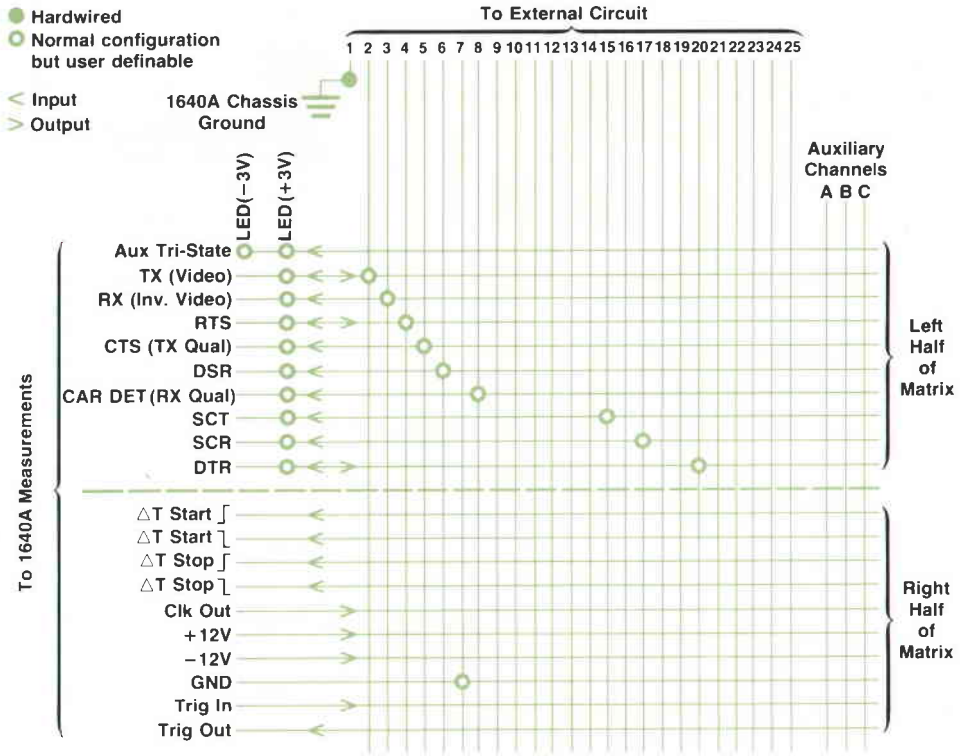


Fig. 5. *Organization of the pin matrix. The 24 leads of the RS-232C bus form the vertical columns and the 1640A inputs/outputs form the horizontal rows. For clarity, the left half of the matrix is shown stacked on the right half.*

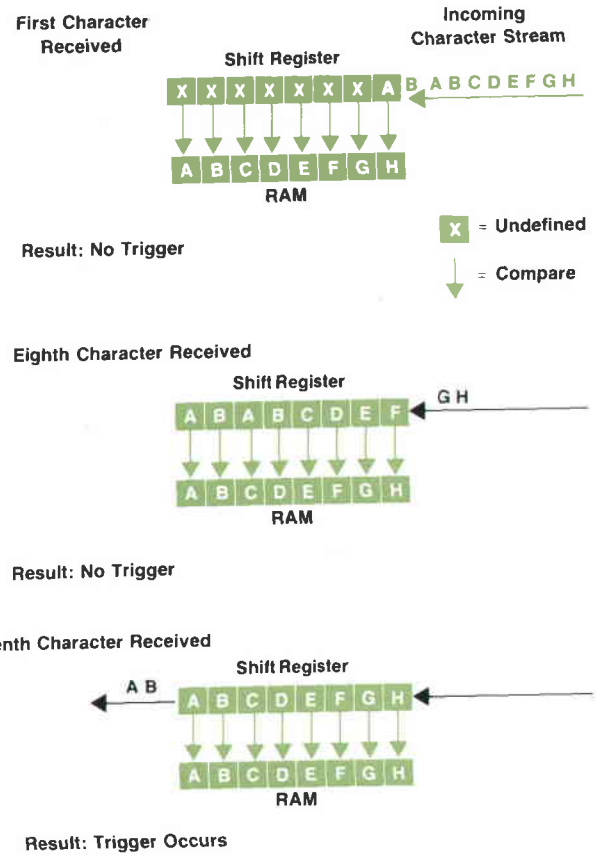


Fig. 6. *Combing of the data stream assures a trigger whenever a trigger sequence occurs in the data stream regardless of what precedes it.*

the user can establish particular pin configurations by punching holes where appropriate.

Flexible Triggering

To effectively troubleshoot and analyze problems on a serial data bus, a data analyzer should be able to capture data in response to a variety of trigger conditions. These should include triggering on specified characters or bit patterns on the transmit or receive lines of the RS-232C bus, triggering on errors such as parity or cyclic redundancy-check errors, and triggering on invalid time intervals such as excessive time between handshake parameters. The 1640A is capable of all of these triggering modes. In addition, it has NOT triggering.

As an example of NOT triggering, let us assume that the response of a terminal to a computer occasionally garbles the fourth character. If the correct response were A B C D E F G H and occasionally the terminal sent A B C ▨ E F G H where ▨ is the garbled character, then the user can trigger on this event without any a priori knowledge of what the garbled character will be. The NOT character is indicated on the 1640A display in inverse video thus:

TRIG A B C D E F G H

This is interpreted as follows:

trigger when A is immediately followed by
B immediately followed by
C immediately followed by
anything but D immediately followed by
E immediately followed by
etc.

Use of NOT triggering thus restricts data capture to those times when a particular sequence contains an error in a particular character.

Data Combing

An important feature of the 1640A's triggering capability is that it performs true combing of the data stream when triggering on character sequences. Suppose that the trigger sequence was defined as A B C D E F G H and that the sequence A B A B C D E F G H appeared in the data stream. This sequence of events might then occur:

1. The first A is detected and accepted as a valid start of a trigger sequence.
2. B is detected. This is a valid second character of the trigger sequence.
3. The second A is detected. This is not a valid third character, so the system starts looking again for a valid first character.

Thus, the first three characters are thrown away because they do not satisfy the requirements for the first three characters in the trigger sequence. This includes the second A even though it satisfies the first-character requirement of the following character sequence. To prevent this, Model 1640A combs the data using a shift-register-RAM technique. As shown in Fig. 6, the trigger sequence is loaded into the RAM during instrument setup. As each character in the incoming stream is detected, the character

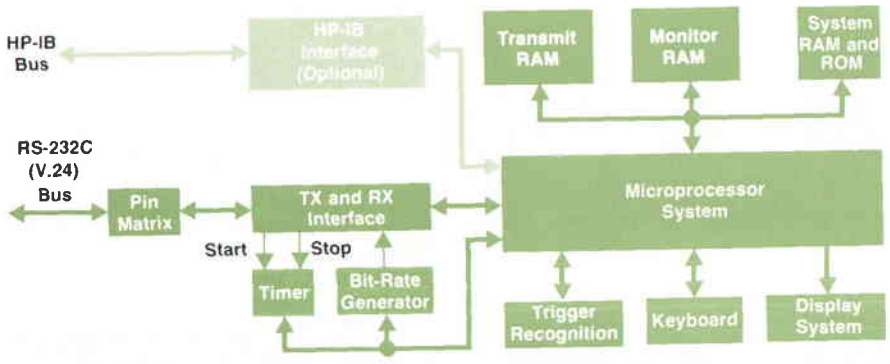


Fig. 7. *Simplified block diagram of Model 1640A. It is microprocessor-based (8080-4), which enables it to perform a wide variety of measurements without a lot of software.*

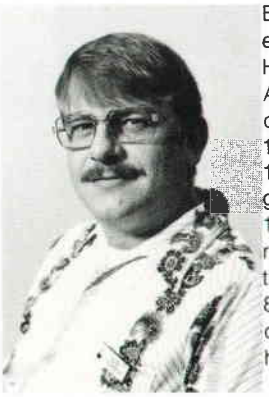
is loaded into the shift register and then shifted left when the next one is entered. Each time a character is entered, the shift register contents are compared to the RAM contents, and when a 100% coincidence is detected, a trigger is generated. No characters are inadvertently thrown away.

Instrument Organization

A block diagram of the Model 1640A is shown in Fig. 7. The interface to the RS-232C bus is by way of two 8251 USARTs (universal synchronous/asynchronous receiver-transmitters). The microprocessor performs real-time data acquisition in software by interleaved polling of the USARTs. The data-acquisition software is all in-line code for speed of execution but most of the rest of the software is table driven.

The trigger recognition circuitry is shown in the block diagram of Fig. 8. For the sake of simplicity, this shows a scaled-down version that works with sequences of four 4-bit characters. Operation is as follows:

1. The specified trigger sequence initially is loaded into



Robert E. Erdmann, Jr.

Bob Erdmann designed radar test equipment for a year before joining HP's Colorado Springs Division in 1969. At HP, he was involved in the design of oscilloscope vertical amplifiers (1805A, 1834A, 1835A) before joining the 1640A project. Bob earned a BSEE degree at Purdue University (Indiana) in 1968. In off hours, he indulges in model railroading, woodworking, and astronomy. He designed and built his own 8-inch Newtonian telescope and his own home computer. Bob and his wife have two children, 8 and 3.

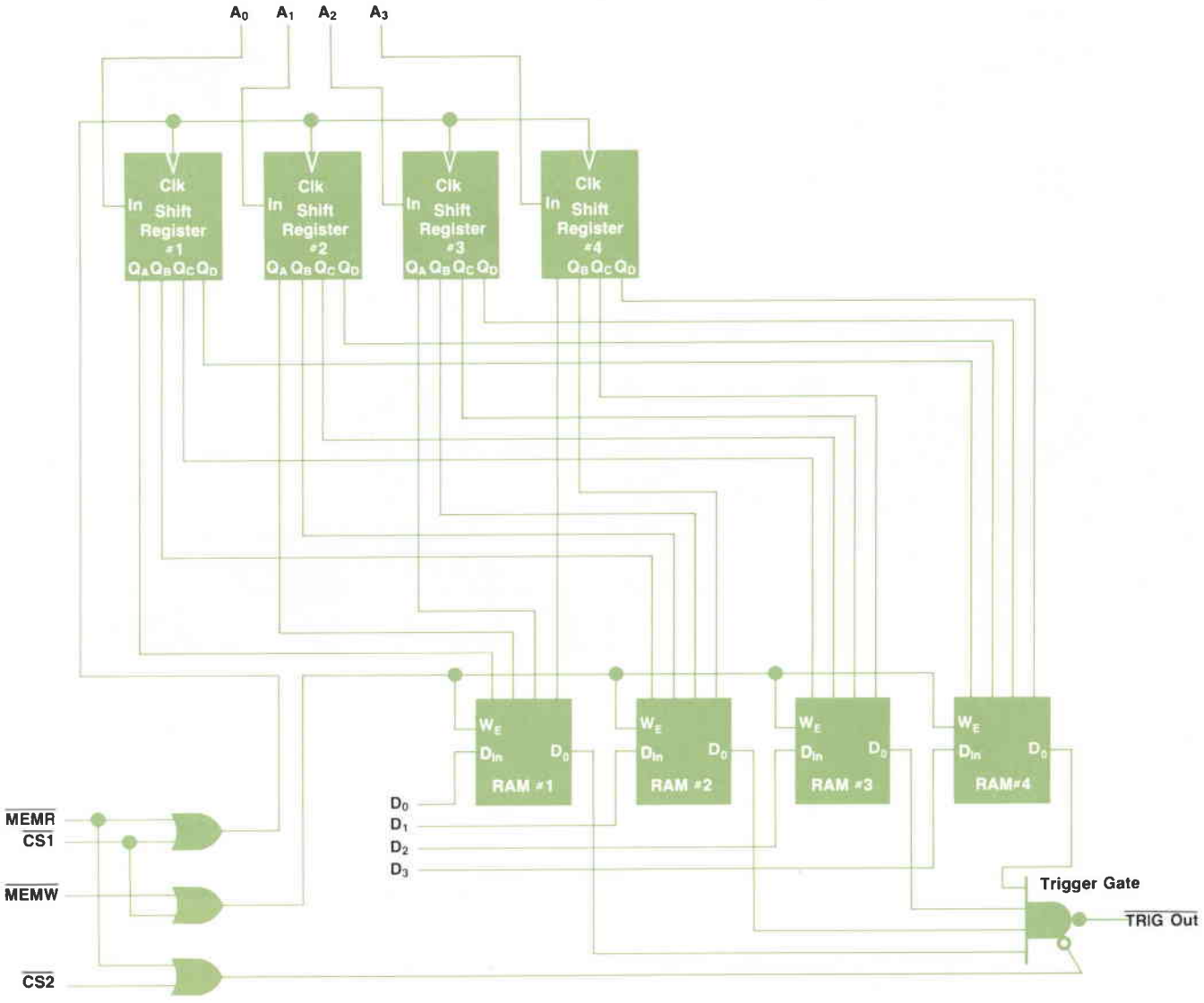


Fig. 8. *Scaled-down representation of the trigger recognition circuitry.*

the shift registers by placing the first four-bit character on the lower four bits of the microprocessor's address lines (A_0–A_3) and executing a microprocessor memory read ($\overline{MEMR}$) from the address of the shift registers ($\overline{CS1}$). This is repeated for the remaining three characters.

2. The outputs of the shift registers (Q_A–Q_D) are connected to the address lines of the RAMs. The bit pattern in the shift registers thus defines a unique address in each of the RAMs. At this time, the microprocessor places ones on all the data lines (D_0–D_3) and does a memory write ($\overline{MEMW}$). The RAMs now contain ones at the addresses specified by the shift register contents.

3. All four-bit sequences except the trigger sequence are now entered into the shift registers and zeros written into the RAMs at the addresses specified by these sequences.

4. When an incoming character arrives, it is placed on the lower four bits of the microprocessor's address lines and loaded into the shift registers. A memory read ($\overline{MEMR}$) is then executed at the address of the trigger gate ($\overline{CS2}$). If all the RAMs have a one at the address specified by the shift register, the trigger gate will then output a one, indicating that the trigger sequence has occurred.

This system also enables NOT triggering and "don't care" triggering merely by appropriate placement of ones on the data lines (D_0–D_3) during the trigger specification sequence at the time that zeros are normally loaded.

Acknowledgments

John Poss was the project leader. Rick Vestal did the hardware design and product design was by Bobby J. Self. HP-IB software was by Dave Novotny, data acquisition software by Paul Sherwood, and system software by the author.

SPECIFICATIONS

HP Model 1640A Serial Data Analyzer

INPUT IMPEDANCE: >30 kΩ on all interface connections except ground.

Format

FRAMING: 5,6,7, or 8 information bits with or without a parity bit.

DATA CODES: ASCII, Hex, or EBCDIC. Other optional code sets in addition to or in lieu of EBCDIC are available.

DATA MODES

ASYNCHRONOUS: 1 or 2 stop bits in addition to information and parity bits.

SYNCHRONOUS: 1 or 2 user-entered synchronizing characters. Sync search may be initiated on a user-entered character immediately followed by a user-entered number of idle characters from 0 to 99. Idle is defined as a steady mark (logic 1's) in all bit positions.

SPEED

EXTERNAL CLOCK (Synchronous)

CHARACTER SIZE INCLUDING PARITY (bits)	NORMAL OPERATION Bits Per Second		HIGH SPEED MODE* Bits Per Second	
	HDX	FDX	HDX	FDX
9	19200	9600	19200	9600
8	14400	7200	19200	9600
7	14400	7200	19200	9600
6	9600	6400	14400	7200
5	9600	4800	9600	7200

*Memory data is not displayed while a run is in progress. High speed switch located on rear of patch panel matrix.

INTERNAL CLOCK (Asynchronous): 50, 75, 110, 134.5, 150, 200, 300, 400, 600, 900, 1200, 1800, 2400, 4800, and 9600 bps, ±1%. Also, any external ÷1 clock to a maximum of 9600 bps may be used for asynchronous operation.

ERROR CHECK: odd, even, or no parity; optional (003) BCC generation and checking based on LRC-8, CRC-16, or CRC-CCITT from a user-entered beginning to a user-entered ending character. Optional (002) SDLC frame check sum (FCS) generation and error checking for SDLC frames.

Triggering (Trap) Modes

CHARACTER SEQUENCE: up to 8 sequential characters including NOT and DON'T CARE may be used as a trigger and may be specified on either the send or receive data lead. NOTE: DON'T CARE is the set of all possible bit patterns of any given character length. The NOT character is the set of all characters except the one specified.

TIME INTERVAL: time intervals between two RS-232C events may be used as a trigger. Maximum or minimum times to 6553 ms with 1-ms resolution may be specified.

ERROR: data errors, as defined in the FORMAT menu under ERROR CHECK, may be used as a trigger.

EXTERNAL: trigger supplied from user hardware or RS-232C ON conditions (>+3V).

Supplemental Characteristics

PATCH PANEL MATRIX: permits the 1640A to be configured to a variety of system interface formats depending on the application. Mylar overlays are provided with prepared pin configurations for common applications to facilitate matrix set-up. An auxiliary, tri-state LED may be used to monitor any pin 2 through 25. The matrix also provides access to the time interval counter, external trigger input, trigger output, clock output, and buffered power supplies (±12 V, ground).

TEST RESULTS: after any of the three run modes (monitor and simulate) is stopped, the following test results are displayed:

1. Last time interval measured, or the time interval trigger event, between user-definable start and stop events available on the patch panel matrix.
2. Number of trigger events counted during the run.
3. Number of messages transmitted by the 1640A (simulate only).

SUPPRESSION: allows capturing only the information of interest for efficient use of memory and easier data analysis. Synchronizing characters, idles (all logic one's), nulls (all logic zero's), or everything but the trigger and the next n characters (with n from 0 to 99) may be suppressed.

Monitor Mode

RUN (EXECUTE) MODES

COUNT TRIGGERS: continuously monitors and records data and counts the number of trigger occurrences; record is stopped manually.

TRIGGER STARTS DISPLAY: trigger starts a single record of 2048 characters (any combination of transmit and receive data).

TRIGGER ENDS DISPLAY: trigger stops a continuous record. A built-in delay of 64 characters captures 64 characters after the trigger event.

Simulate Mode

The 1640A can simulate a CPU, terminal, or the digital side of a modem.

OUTPUT: >3 V into 3-kΩ load. Output rows on the patch panel matrix are TX (Transmit Data), RTS (Request to Send), and DTR (Data Terminal Ready).

INTERFACE CONTROL SIGNALING: automatic with additional control available through the matrix.

STATE: ON is >+3 V; OFF is <−3 V. Nominal values of driven leads are ±8V to ±12 V.

HDX: REQUEST TO SEND is on only during transmission.

FDX: DATA TERMINAL READY is always on; REQUEST TO SEND is programmable via the matrix, either always on or on only during transmission. Idle condition between transmissions is a steady mark (asynchronous) or the user-entered sync character (synchronous).

REPLY ON: similar to, but separate from, trigger. A REPLY ON sequence of from 1 to 8 characters, including DON'T CARE and NOT characters, immediately followed by an internally generated time delay from 0 to 6553 ms may be entered; this enables a message block to be sent only when these two events occur.

RUN (EXECUTE) MODES

SINGLE AND COUNT TRIGGERS: a message block is transmitted after each occurrence of the REPLY ON condition until all message blocks have been sent once. The run automatically stops when a total of 2048 characters (including the transmitted message) have been recorded in the monitor buffer.

REPEAT AND COUNT TRIGGERS: a message block is transmitted after each occurrence of the REPLY ON condition until all message blocks have been sent. The process repeats until manually stopped with the last 2048 characters retained in memory.

REPEAT AND END ON TRIGGER: a message block is transmitted after each occurrence of the REPLY ON condition until all message blocks have been sent. The process repeats and automatically stops when the trigger event occurs with the last 2048 characters prior to the trigger event retained in memory.

TRANSMIT MODES

TRANSMIT FIRST: the first message block is sent by pressing RUN. Succeeding blocks are sent following each occurrence of the REPLY ON condition.

RECEIVE FIRST: a message block is sent after each occurrence of the REPLY ON condition.

TRANSMIT MESSAGE ENTRY: a total of 1024 characters including block delimiter continue symbols (|→) and the end symbol (|—), may be entered. The transmit memory may be loaded thought the hex keyboard, by transferring the contents of the monitor memory to the transmit memory with a single keystroke, or, with Option 001 (HP-IB), through a remote ASCII keyboard or user-definable PROMS (1029A).

MESSAGE EDITING KEYS

CONTINUE: places a |→ symbol in the message as a block delimiter. Up to 10 continue symbols may be entered. The continue symbol is recognized only by the 1640A and is not sent as part of the data.

END: places a |— symbol as a message terminator. Additional messages may be added after the end symbol as user instructions but will not be transmitted. The end symbol is not sent as part of the data.

INSERT: inserts a space for an additional character at the point indicated by a movable cursor by automatically shifting all following characters one cell to the right.

DELETE: deletes the character immediately above a movable cursor. All following characters are automatically shifted one space left.

General

MEMORY: 2048 characters of monitor buffer and 1024 characters of transmit message buffer.

POWER: 100, 120, 220, 240, Vac; −10% to +5%, 48 to 440 Hz; 150 VA max.

DIMENSIONS: 251 mm H x 335 mm W x 445 mm D (9 7/8 x 13 3/16 x 17 1/2 in).

WEIGHT: 11.4 kg (25 lb).

OPERATING ENVIRONMENT

TEMPERATURE: 0°C to +55°C.

HUMIDITY: to 95% relative humidity at +40°C.

Options

001: HP-IB Interface*

002: SDLC (Synchronous Data Link Control) /HDLC (High Level Data Link Control) Interface*

003: LRC, CRC-16, and CRC-CCITT Check/Generation*

H07: Adds capability for up to five additional internal code sets.

*Field installable. Options 002 and 003 reside in the same location so cannot be installed simultaneously.

PRICES IN U.S.A.: Model 1640A, $5800. Opt 001, $475; opt 002, $200; opt 003, $150; H07, $100 (check nearest HP field office for price of code-set ROMs).

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