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A Computer-aided Hospital System for Cardiac Catheterization Procedures

Computer reduction of data acquired during cardiac catheterization eliminates considerable pencil and paper computation, a significant time-saver for the physician. Simultaneously, it guarantees highly sophisticated measurements while shortening a normally lengthy procedure, a less disquieting experience for the patient.

By John L. Fanton

MEDICAL DATA ACQUISITION SYSTEMS solve the problem of gathering meaningful information from a multitude of sources rapidly but, like their counterparts in industry, they very often create a new problem—how to digest all that data.

Cardiologists at the Stanford University School of Medicine are among those being buried under an avalanche of system-acquired data. With highly complex medical procedures such as cardiac valve replacement and organ transplants becoming widespread, large amounts of data are being generated either during the operation itself or during the patient preparation phase or 'work up.'

One procedure contributing significantly to this glut of information is cardiac catheterization. A typical catheterization procedure may take up to four hours to complete, and it generates graphic records that require at least one and as much as three hours to reduce to useful form.

Making sure that the acquired cath lab data is meaningful presents an additional problem of some magnitude. While concerned with other duties, the cath lab technician may operate the strip-chart recorder incorrectly. Or, the data might be obscured by interference introduced by the catheter's position. Additionally, there could be transient equipment failure.

To assure that all the needed data is acquired and that this information is correct, measurements are often repeated. This introduces the most important problem of all—the comfort and safety of the patient. Thus, automatic data reduction is desirable not only for saving time in the data reduction phase, but, by directly presenting the physician with measurement results while the catheters are in place, for reducing significantly the time the patient needs

to be in the cath lab. At the same time, this immediate display of measurement results would permit more sophisticated investigations.

The Cardiology Division of the Stanford University School of Medicine therefore undertook the development of software for on-line analysis of data acquired during a catheterization procedure. Hewlett-Packard later joined them to develop a complete system for computerizing the data reduction. This effort has resulted in the HP Model 5690A Computerized Cardiac Catheterization Laboratory System.



Cover: Keyboard and monitor give nurse/technicians control of computer in new computerized cath lab measurement system. Readily integrated into existing procedures, system greatly speeds up interpretation of data acquired during cardiac catheterization. For an account of how this system evolved, read the article beginning on this page.

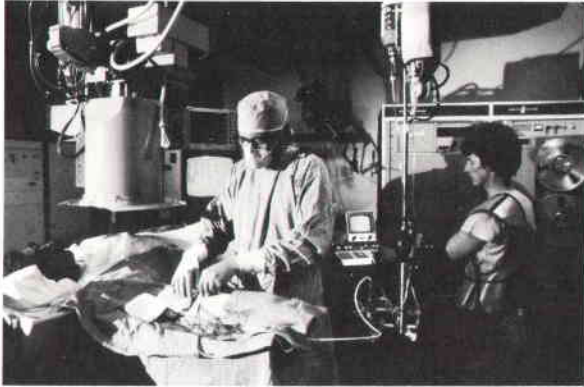
In this Issue:

A Computer-Aided Hospital System for Cardiac Catheterization Procedures, by John L. Fanton **page 2**

Clip-and-Read Finds IC Failures, by Mark Baker and Jesse Pipkin **page 8**

The Well-Modulated Synthesizer, by James E. Stinehelfer **page 13**

The Cath Lab



Faulty valves and other defects in the heart's hydraulic operation — ailments once considered irremediable — can now be corrected with recently developed open-heart surgical techniques. And with the growing practice of open-heart surgery has come an increase in cardiac catheterization procedures, for this is where the real nature of the heart's defects are defined.

Cardiac catheterization consists of inserting a thin, flexible, plastic tube (the catheter) into a vein or artery in either an arm or leg and sliding it in until it reaches the chambers of the heart. Recordings of the dynamic pressures in the chambers of the heart and nearby arteries may then be made since pressure at the tip of the catheter is hydraulically coupled to an external pressure transducer through a saline solution that fills the catheter or measured at the tip by tiny solid-state transducers. The same catheter may also be used for drawing off blood samples at selected points in the circulatory system. The patient's ECG is also recorded, primarily to provide a time reference for comparing the phases of pressure waveforms recorded at different times.

From the information gathered during the catheterization

procedure, the physician can determine pressure gradients across valves, cardiac output, vascular resistance and other factors that indicate precisely the position, size, and degree of cardiac abnormalities. Very often two or possibly three catheters, inserted through separate blood vessels, are used so that two or more pressures may be recorded simultaneously to provide measurements of pressure differentials.

Catheterization is performed only when thorough examination by non-invasive techniques (X-rays, electrocardiography, heart sound analysis, blood chemistry analysis, etc.) indicate that catheterization is absolutely necessary. It is a tricky procedure as the catheter tip may not always follow the intended path, calling for considerable backing off, twisting, and probing, especially when guiding the catheter past one or more of the heart's valves. The physician monitors the progress of the catheter with a fluoroscope. He also watches the pressure waveforms on a large-screen monitor because the nature of the waveforms assist him in making judgments about catheter tip positioning.

The cath lab procedure may take two or more hours. The patient receives only a local moderate anesthetic since measurements are made both in the resting state and during exercise (cath lab equipment includes a bicycle-pedal exerciser that can be used while the patient is lying down).

The end result of a cath lab procedure is 20 feet or more of oscillographic recordings of pressure waveforms, and a listing of chemical analyses performed on the blood and respired air. The physician must then spend two or more hours analyzing the data. He reduces the data by first measuring the peaks, valleys, and gradients of the waveforms. These numbers are then used for the calculations required to get the desired information.

With the computer system described here, these calculations are performed on-line during the catheterization procedure. This shortens the time the patient needs to be kept in the cath lab, since immediate availability of the calculated data can guide the course of the cath lab procedure, all the while assuring that the necessary data is acquired. It also reduces the physician's workload by a significant factor, leaving him more time for direct patient care.

Meeting Medical Needs

Objectives mutually agreed upon at the beginning of the system development included:

- Computer results must be presented in a form useful to the physician.
- No constraints should be placed on the accepted cath lab procedure because of the computer.
- The system should not require additions to the cath lab team.
- Computer failure must not compromise the procedure.
- The cost of the system should be commensurate with the time saved.

Fortunately, the Stanford Cardiology Division was able to provide a clinical environment for system evaluation. HP engineers, after a literature study of cardiac physiology and disease, spent a number of weeks in an operating cath lab observ-

ing what the system operating environment is, what each member of the team does, and what the individual stress levels are. Considerable time was spent with each member of the catheterization team to determine how a computerized system could improve the existing manually-handled procedures. From this, a computerized cardiac catheterization system evolved, a system that is easily used by medical personnel who do not have a computer background.

The System

The computerized cath lab system is actually comprised of two systems: an analog measurement system and the computer system (Fig. 1).

The analog measurement system includes the pressure transducers and ECG electrodes, suitable medically-oriented preamplifiers, a large-screen dis-

play for the waveforms, and an optical strip-chart recorder. It feeds the analog waveforms to an analog-to-digital converter for use by the computer.

Although the preamplifiers were modified to allow automatic calibration in response to computer commands, the analog system can still be used by itself to make cath-lab measurements in the traditional non-computerized manner. This allows the smaller hospital to equip a cath lab with the analog system alone, and then to add the computer system when increased cath lab usage warrants.

The computer system can be either of the HP Disc Operating Systems: the DOS fixed-head disc system, or the DOS-M Moving-Head Disc System (a little slower but less expensive). Neither of these software executives were modified, allowing the computer to be used for other tasks when the cath lab is not in use.

The Gist of the Problem

Hardware development centered on the man-machine interface, in many ways the most difficult part of the development to define. Stanford personnel had previously determined that the traditional teletype interface is unsuitable for the cath lab because the noise could be disturbing and its operation would be too time-consuming for those who do not have a computer background. What was desired was a calculator-like keyboard that could process data according to directions imparted by the simple push of a button.

As a result of this need, a special-purpose keyboard was designed. The first prototype is shown in Fig. 2(a). It has special computation keys along the bottom and a typewriter-style keyboard that lets the nurse/technician enter notes during a procedure, obviating the need for making entries in the protocol log book.

A few weeks' experience in the cath lab disclosed that the typewriter keyboard was impractical. Few technicians are accomplished typists and the necessity for darkening the room during X-ray procedures prohibited 'hunt and peck' typing. The same trial period also disclosed problems with the grouping of the computation keys. Nurses often had trouble finding certain keys at critical moments.

So, back to the drawing board. A second keyboard evolved. As shown in Fig. 2(b), the typewriter keyboard is eliminated and the computation keys are grouped into blocks according to function. Frequently used keys are on the corners of the blocks where they can be found easily by touch. This keyboard came much closer to fulfilling the goal of usefulness without special training.

From discussions with the staff using this keyboard, further refinements were made. The resulting third prototype, Fig. 2(c), became the final design when trials for this keyboard showed that it fulfilled all objectives and required only a brief familiarization period.

Interaction

Cathode-ray tube display of data and intermediate program steps closes the operator loop to give full interactive operation with the computer. CRT display was chosen because of its speed, versatility, and absolute silence.

To avoid adding equipment to the laboratory, it was decided to display the data on the same TV monitor used for the X-ray image intensifier. The monitor is installed where the physician can view it without moving from the catheterization table and, because it displays an image only when the X-ray system is turned on, it is available for data display during the measurement periods.

Subsequent observations indicated that the monitor was not in a position where the recording technician could watch the monitor while selecting keys, so a small monitor was added at the keyboard.

The system still includes a teletype, but this is installed in the computer room where it is used for entering off-line data such as patient identification number, name, weight, etc. It also prints a hard-copy report at the conclusion of the cath lab procedure.

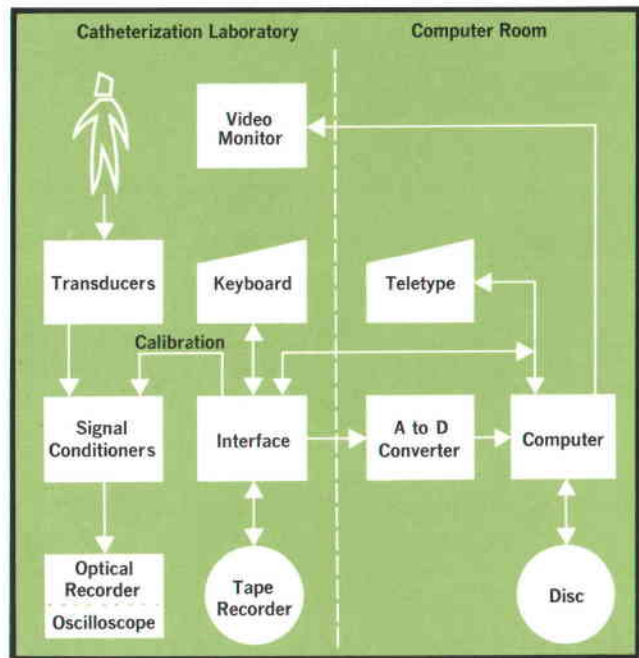


Fig. 1. Typical configuration of cath lab system.

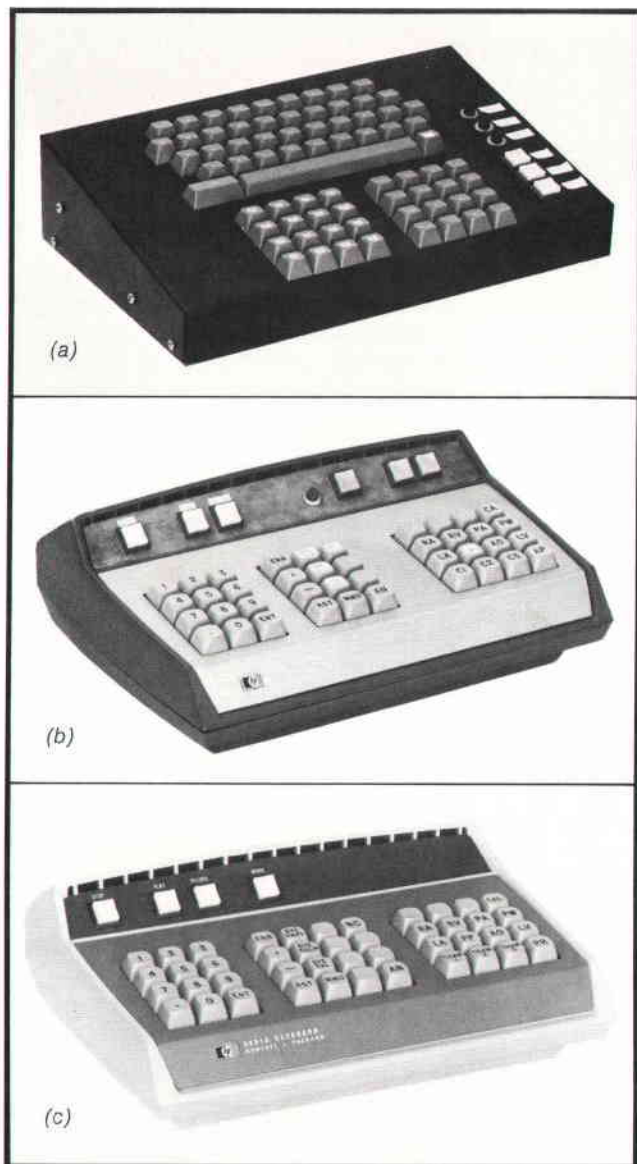


Fig. 2. Keyboards trace system development. First prototype (a) had calculator-like function keys plus alphanumeric keyboard. Alphanumeric section, found to be superfluous, was deleted from second prototype (b). Further refinements in key arrangement were made in final prototype (c). Blank pushbuttons are for functions that may be added as more elaborate procedures are developed.

Straightforward Commands

Software, based on the Stanford-developed Fortran programs, was designed with the nurse/technician staff in mind. Wherever possible, control codes were based upon accepted abbreviations for medical terms. For example, LA and RA indicate left atrium and right atrium respectively. Actually, the software includes some twenty independent programs that can be called up in any order accord-

ing to the keyboard commands. This allows the physician wide latitude in selecting the order in which measurements are to be made.

Substantial time was spent making sure that no combination of keyboard commands could abort the system. One worthwhile feature that was added is a RESET command. It had been noticed that under a high-stress condition the operator could become confused part way through a sequence of commands and become completely lost. The RESET command returns the program to an easily recognized point, allowing the operator to start again.

Uninterrupted Data Flow

To insure no loss of data, system backup received considerable attention. The analog system provides a first-level back-up for possible computer failure because it can continue to generate records for manual reduction.

A second back-up is provided, however, in the form of a mag tape recorder. This not only records the analog signals, but it also records coded signals in response to the keyboard commands. When the computer is up again, the tape can be replayed into the computer. The computer then reduces the data immediately under control of the recorded commands. (The tape system also records comments by the technician on a voice track.)

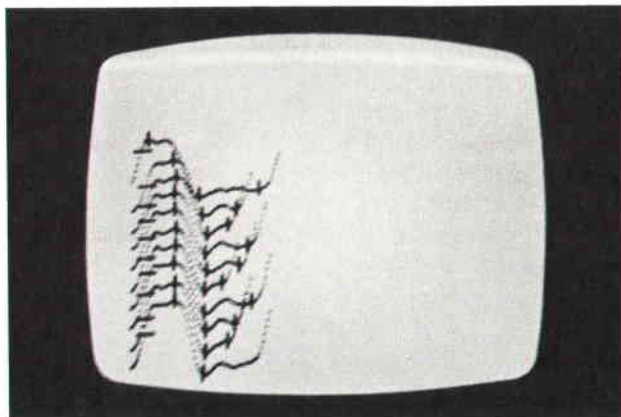
Economical in its Way

Improved patient care could justify this system without economic considerations, but hospitals do not have unlimited funds and must consider economics when allotting resources. The economics of this system can be interpreted in terms of time saved for the physician. If his time is valued in a range of \$20 to \$40 per hour, a cath lab doing two procedures a day can save about \$30,000 a year, a significant amount in light of the cost of a typical system (\$67,000). A new version of the system using the HP Real-Time Executive will allow up to four cath labs to share one computer, reducing unit costs even further.

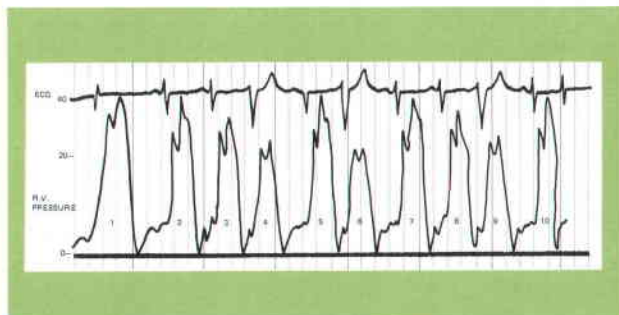
Field Proven

The prototype system at Stanford has been operating for over a year and has been used on more than 250 patients. Comparisons of computer-derived results with those of cardiologists working in the traditional manner show excellent agreement, establishing this system as a worthwhile addition to the tools required by a sophisticated cardiology department.

Finding a Good Waveform



Pressure waveforms retained in computer are re-created for display within seconds of analog waveform sampling. Markers show points selected for calculations (e.g. peak systolic pressure, beginning diastolic pressure, end diastolic pressure, dp/dt, etc.).



Analog recording of ECG and typical pressure waveform.

The algorithms for reducing raw physiological waveforms to meaningful information were developed mostly by members of the Stanford University School of Medicine's Cardiology Division. The problems inherent with physiological signals, mainly low signal-to-noise ratios and variable signal quality, required rather complicated decision criteria to identify points of interest.

In response to an operator command, the system's A-to-D converter samples a waveform at a 100-Hz rate. Sampling continues until the system has counted 11 heartbeats derived from the ECG. Because of uncertainties in the beginning and end of a pressure waveform, data from the first and last beats are discarded, insuring that all 9 of the remaining beats are complete cardiac cycles.

The samples are passed through a digital filter³ to remove noise. The filter numerically convolves each sample with an 11-point weighted average. The filtered data is then stored on the disc memory for later analysis.

When analysis is requested, the system first checks the anatomical site being measured and then selects the appropriate algorithm. The analysis is beyond the scope of this article but it involves decision criteria based on time, amplitude, and rate of change.^{4,5} After analysis, the reconstructed waveforms are displayed with marks to indicate where waveform values are to be chosen, e.g. peak systolic and diastolic pressures.

To further reduce anomalies, the chosen values of all nine cardiac-cycles are rank ordered. The middle-three values are then averaged to obtain the reported value, the upper three and lower three being ignored. This removes abnormal beats, such as those caused by pre-ventricular contractions which result in one beat with abnormally high pressure and one with abnormally low pressure. The value reported is thus truly representative. The system then computes values for valve gradients, valve areas, cardiac output, stroke volume, systolic ejection period, diastolic filling period, and any other called parameters.

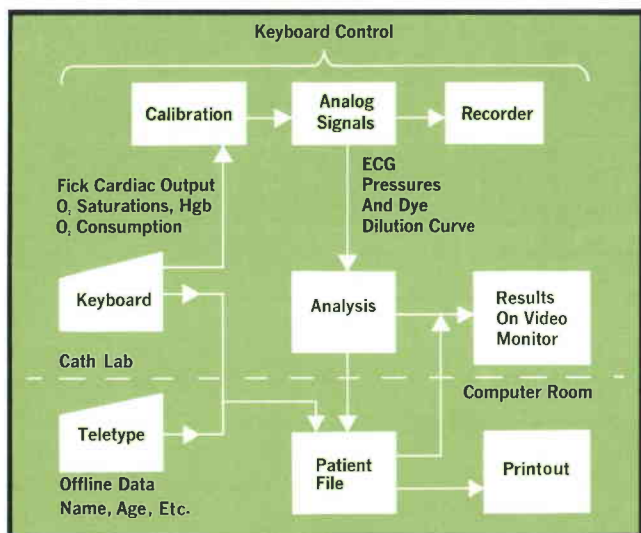


Fig. 3. Information flow.

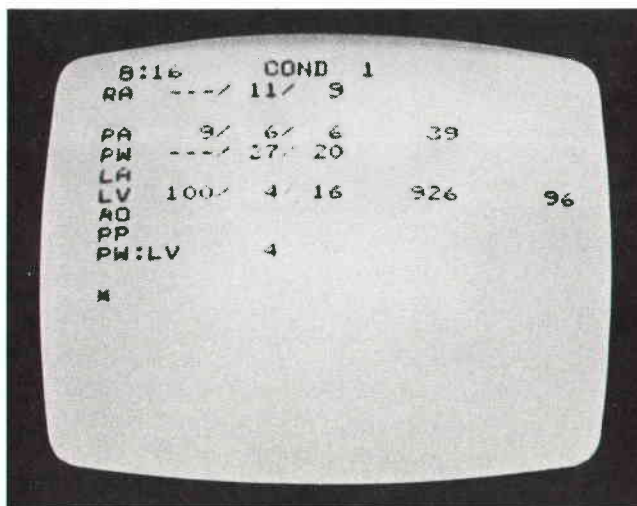


Fig. 4. Monitor displays calculations called for during catheterization procedure.

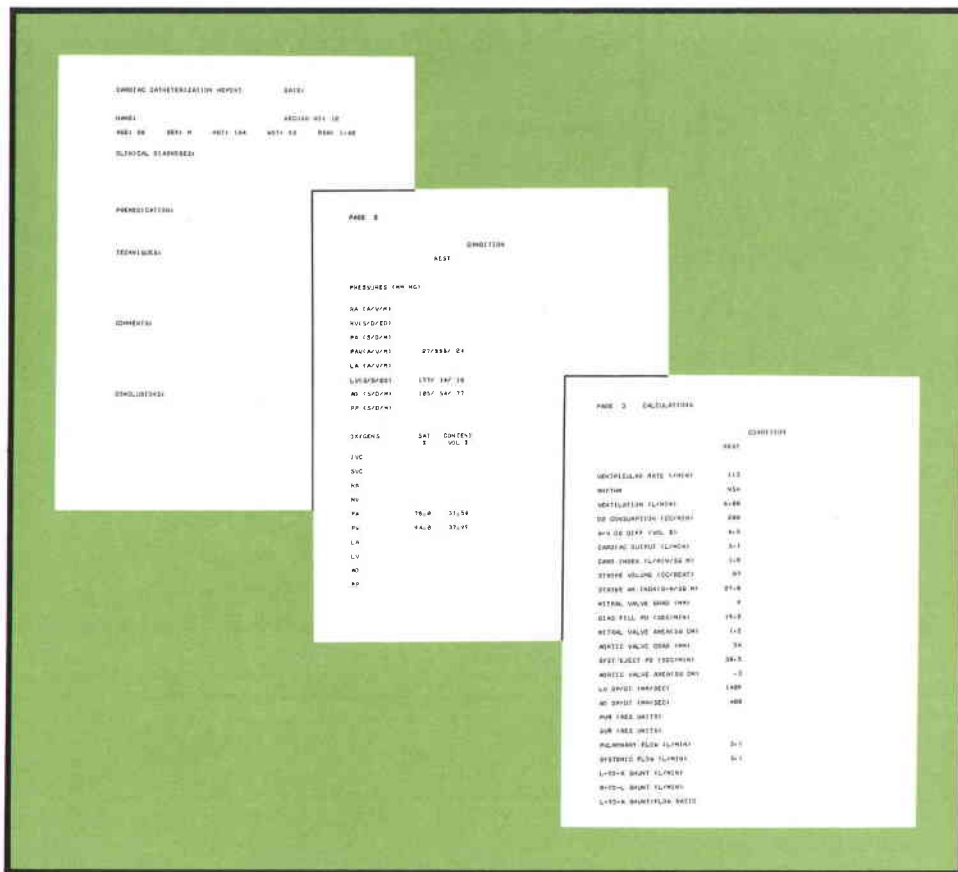


Fig. 5. Computer prints out three-page report at conclusion of catheterization data.

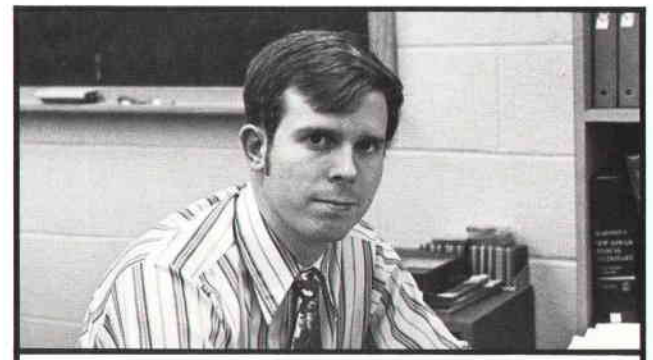
Acknowledgments

The author wishes to express great appreciation to the Division of Cardiology of Stanford University for their guidance, particularly to Dr. Donald Harrison and Mr. William Sanders without whose help the Computerized Cardiac Catheterization Laboratory System would not be a reality. Thanks are also extended to Richard Regan for his work on the keyboard and control section.

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John L. Fanton

With BSEE and MSEE degrees from Cornell in hand, John Fanton joined Hewlett-Packard's Medical Electronics Division in 1968. Initially he worked on the design of a single-channel ECG recorder for nurses' stations and then went on to the world of multichannel systems and computers as project leader for the Computerized Cath Lab System. John is married and, with but one child so far, he still has time for skiing, photography, and music.

Clip-and-Read Comparator Finds IC Failures

Here's a clever new tool for troubleshooting digital integrated-circuit equipment.

By Mark Baker and Jesse Pipkin

You probably wouldn't use a sledgehammer to crack a walnut. Or a scrub brush to clean your teeth. Or (usually) an oscilloscope to measure voltage. In these and countless other tasks, doing an efficient job is largely a matter of choosing the right tool. Until recently, however, when it came to troubleshooting digital integrated circuits in design, production, or service, the right tool just didn't exist. There was no alternative to tedious and expensive methods involving manuals, sche-

matics, specifications, oscilloscopes and voltmeters—methods that could only be applied by someone with a high level of technical skill.

The situation is different now. Model 10529A Logic Comparator, Fig. 1, may well be the right tool for finding a digital IC failure. It's a simple, inexpensive, hand-held device that quickly identifies a faulty IC and tells which pins have failed.

Fig. 2 shows how the comparator is used. For an unskilled person the method is fast and nearly

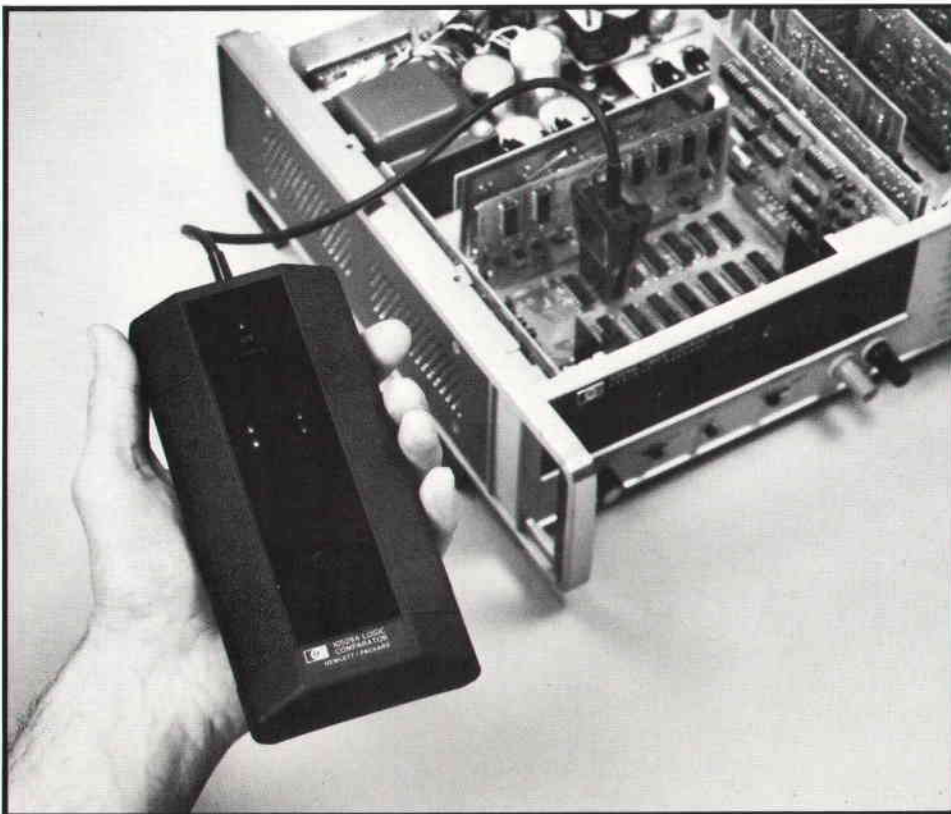


Fig. 1. Model 10529A Logic Comparator finds faulty TTL or DTL integrated circuits quickly and easily. It's self-powered, adjustment free, and requires little training.

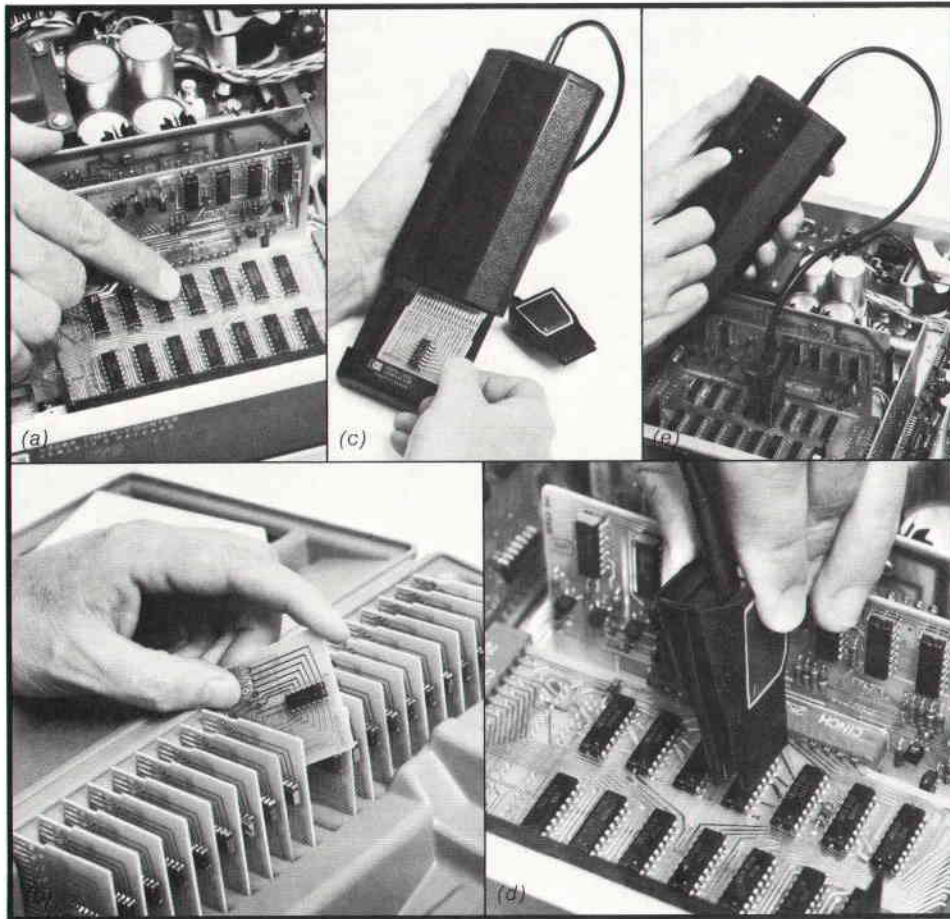


Fig. 2. Here's how to use the logic comparator. (a) Select the IC to be tested and read its number. (b) Select a reference board containing a good IC with the same number. (c) Insert the reference board in the comparator's drawer. (d) Attach the clip to the IC to be tested. (e) Look at the display. The 'ON' light comes on if the clip is properly attached. Any other light indicates an output pin of the IC being tested which doesn't act like the same pin of the reference IC.

foolproof. For someone with experience or training it may be still faster, since such a person will be able to deduce the likely problem area before testing. In many cases the comparator finds failed IC's an order of magnitude faster than other methods.

How It Works

Comparator operation is as follows: select the IC to test, put a similar IC in the comparator's drawer, attach the clip to the IC, and watch the results. The comparator displays any logic-state difference between the test IC and the reference IC.

When the comparator is clipped onto a test IC, the inputs of the reference IC are tied in parallel with those of the test IC. The outputs are allowed to respond separately. The necessary connections are made on the small board that contains the reference IC (Fig. 2b). On this board, traces are broken to identify output pins of the test and reference IC's. V_{cc} and ground connections are also made on this board to supply power to the comparator. This is done by bending and soldering the V_{cc} and ground pins of the reference IC to the V_{cc} and ground buses (Fig. 3). Thus the comparator draws its power from

the power supply of the circuit under test.

Sixteen light-emitting diodes (LED's) are used in the comparator as fault indicators. Each LED corresponds to a pin on a fourteen- or sixteen-pin dual-in-line package. A lighted diode indicates an error at the corresponding pin. Even a very short error (200 nanoseconds or greater) is stretched enough to be easily detectable.

An indication that the clip is placed on the test IC in the proper orientation is given by a seventeenth LED. The comparator is protected against damage that might occur if the clip were placed on the test IC improperly.

Circuit loading is minimized by the use of low-power circuitry within the comparator. Outputs of the IC under test see only one low-power load. Outputs of other IC's that drive inputs of the test IC are loaded by a maximum of 1.2 additional standard TTL loads.

In-House Applications Abound

How useful is the logic comparator? Hewlett-Packard's own experience is revealing.

A number of production lines have found the

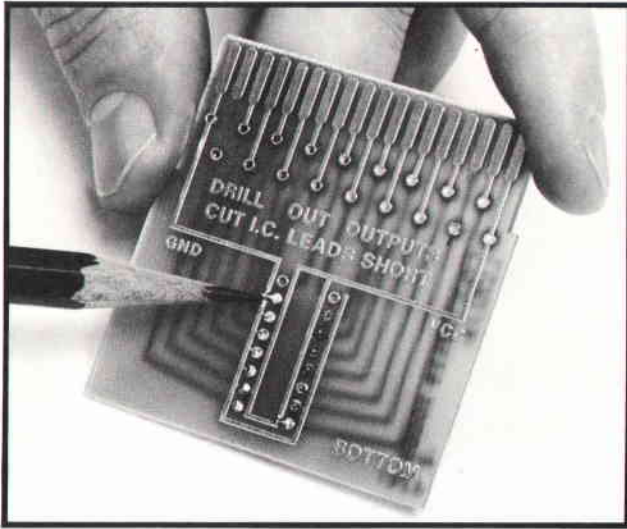


Fig. 3. Output pins are identified by drilling holes in the reference board. V_{cc} and ground connections are also made on this board to supply power to the comparator.

comparator invaluable for isolating failures in shift registers, decades, and other logic IC's. It is used as the primary troubleshooting aid for the 5505A Laser Interferometer Display Unit. The 5360A Computing Counter production line has found it to be nearly indispensable. In the IC-counter areas, the comparator isolates problems ten times faster than conventional techniques. Users may disagree on just how much time the comparator saves but all agree that even the least skilled personnel can isolate IC failures knowing very little about the circuitry. Of course, being able to specify the general area of failure—knowledge gained from experience—speeds up the process, but anyone who can read the identification numbers on the IC's can quickly check every TTL and DTL IC in a circuit.

The logic comparator also locates solder bridges and other improper connections. If an output is held high or low by a shorted lead, it will appear as a failure; thus a failure indication on the comparator locates these stray misconnections.

Two situations require special treatment. When wire-AND connections are used, an output is constrained to be different from what one might expect from observing the inputs of the test IC. The comparator will locate this discrepancy and the user can then refer to the circuit schematic to determine that no failure exists. Shorts inside an IC input, always difficult to isolate, are detected by the comparator as a failure in the driving IC.

The Hewlett-Packard service organization is now incorporating troubleshooting with the logic comparator into HP service manuals. Extensive pro-

grams involving the 5360A Computing Counter and the 5401B Multichannel Analyzer are now underway to evaluate the comparator's impact on the entire concept of field servicing. Several service managers see an eventual end to the expensive and cumbersome spare-board concept and envision instead a portable IC in-circuit tester as the major component of the field service kit. After locating the general area of failure, the repair technician would test the suspect IC's in much the same way that television tubes are tested, except that it isn't necessary to remove the IC's from the circuit.

In the laboratories, HP engineers are also using the comparator. A major benefit is its ability to spot errors that occur at such low repetition rates that they would be difficult to see with an oscilloscope. In some cases, methods of using the logic comparator are being included in new-instrument test specifications released to production.

What Makes It Tick

The logic comparator consists of sixteen identical circuits and a reverse-polarity protection circuit. Each of the sixteen circuits consists of an exclusive-OR circuit followed by a pulse stretcher and an LED driver (Fig. 4). All integrated circuits are of the low-power variety except the NOR circuit which serves as the LED driver.

An output of the reference IC is connected to one input of the exclusive-OR circuit and the corresponding output of the circuit under test is connected to the other input. Any time there is a difference between the inputs of the exclusive-OR circuit, point A goes to a logical '1' state. This forces the output of the NOR gate (point C) to a logical '0' state and turns on the LED through the current-limiting resistor. Each time point A goes to a '1' state, point B also goes to a '1' state for 100 ms.

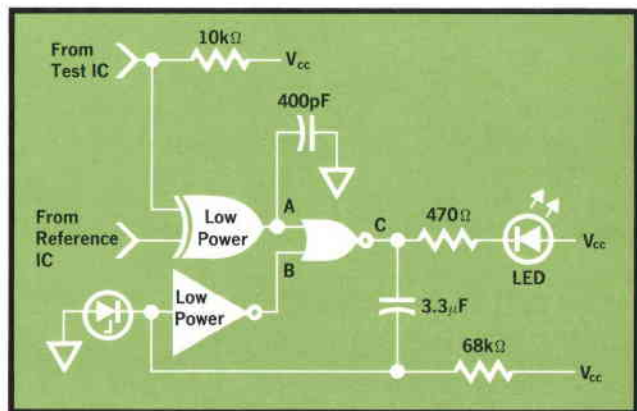


Fig. 4. Sixteen of these comparator circuits compare the test and reference IC's pin by pin.

Probe, Clip, Comparator—Three Complementary IC Logic Testers

The new 10529A Logic Comparator is the third in a series of low-cost, easy-to-use tools designed specifically for testing TTL and DTL digital integrated circuits. Model 10525A Logic Probe¹ checks the dynamic behavior at individual pins. A light at the probe's tip indicates a high or low logic state and a pulse stretcher catches pulses as short as 25 nanoseconds and gives a 0.1-second visual indication. Model 10528A Logic Clip² is a self-powered device that clips onto fourteen- or sixteen-pin dual in-line IC packages and displays the states of all pins on two rows of light-emitting diodes. Probe, clip, and comparator complement one another and enhance one another's value. Model 5010A Logic Troubleshooting Kit contains all three. They're also available separately.

References

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2. 'Deftly Designed—The Logic Clip,' *EDN*, Mar 1, 1970.



Model 5010A IC troubleshooting kit contains a 10525A Logic Probe, a 10528A Logic Clip, and a 10529A Logic Comparator.

This 100 ms is the time required to charge the 3.3 μ F capacitor to 1.4 V (TTL threshold) through the 68 k Ω resistor and the inverter input impedance. Fast recovery time in the stretcher loop is obtained by means of the Zener diode which limits the maximum voltage between the inverter input and ground to 3.16 V. The 400 pF capacitor on the output of the exclusive-OR circuit is used to slow down its response to make it immune to short

error indications caused by different propagation delays in the reference IC and the circuit under test.

Self-Test

Since the comparator is a troubleshooter for other instruments, it's especially important that the user have confidence in it. For this reason a self-check board is included with each comparator (Fig. 5). The test board is plugged into the reference slot of the comparator and is powered by 5 V from any laboratory power supply.

The self-check board has two test modes. The first mode exercises all the comparator's electronics and the LED indicators. The test is completed by observing that all LED indicators blink in unison at approximately 1 Hz when the test board is inserted and +5 V is applied. This test exercises the comparator with various input combinations including the case of a very short fault which requires the pulse-stretching capability.

The second test mode checks for continuity from the clip through the cable to the comparator. This test is made by connecting the clip to a dummy IC on the test board and observing the LED's blinking in unison at approximately 2 Hz. If one wire in the cable is discontinuous, the LED corresponding to that pin position blinks at one-half the rate of the LED's surrounding it.

The test board delivers two waveforms to the logic comparator. One waveform represents signals coming from the reference IC and the other represents the waveform coming from the circuit under test. The combination of these waveforms gives a complete check of the comparator. In the cable-test check mode, the clip is placed on an IC with all pins connected to ground. This grounding of the clip eliminates (grounds) one of the waveforms and

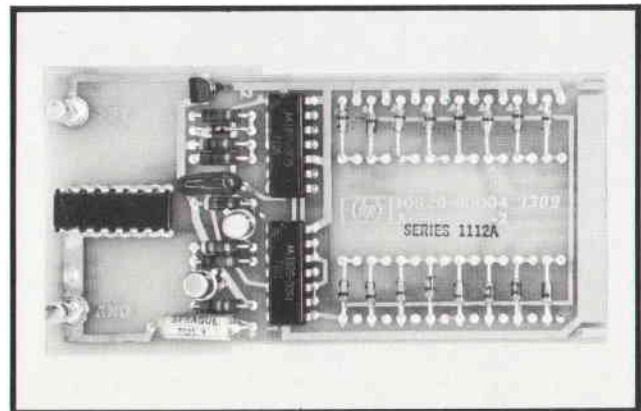


Fig. 5. Self-check board is inserted in the comparator's drawer to make sure the comparator is functioning properly.

hence changes the display. Any broken wire would therefore show up as having a blinking pattern unchanged by the grounding of the clip.

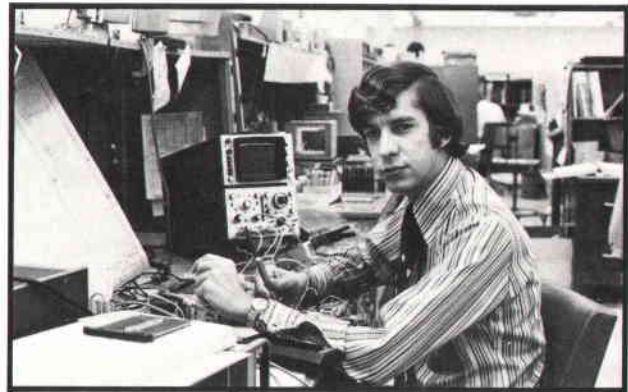
The test board produces the waveforms by gating signals from a counter and one of its differentiated outputs. The differentiator supplies the pulses necessary to test the pulse stretchers. The counter is clocked by a unijunction-transistor relaxation oscillator.

Mechanical Design

The logic comparator is designed for heavy use. An aluminum extrusion serves as a one-piece case, board support, and reference-drawer guide. Easy insertion of the reference card is accomplished by a plastic molded drawer mechanism which accepts the reference board and guides it into its connector.

Acknowledgments

The industrial design of the logic comparator is by David Goelz and James Hergert. Initial feasibility was proved by Gary Gordon and Jon Garman. Roy Criswell smoothed the road to production.



Mark Baker

Mark Baker's a project manager in the logic test section at HP's Santa Clara Division. He received his B.S. degree in electrical engineering from Oklahoma State University in 1969 and his M.S.E.E. from Stanford University in 1970. At HP, starting in the summer of 1969, he's designed the 10528A Logic Clip and contributed to the design of the 5525A Laser Interferometer System and the 10529A Logic Comparator. Obviously (logically?) an outdoor enthusiast, Mark puts water skiing, tennis, and hunting at the top of his list of preferred activities.

SPECIFICATIONS

HP Model 10529A Logic Comparator

INPUT THRESHOLD:

1.4 V nominal, TTL or DTL compatible.

TEST IC LOADING:

IC driving test IC inputs loaded by 2 low-power TTL loads plus input of Reference IC. Test IC outputs loaded by 2 low-power TTL loads.

INPUT PROTECTION:

Voltages < -1 V or > 7 V must be current limited to 10 mA.

SUPPLY VOLTAGE:

5 V $\pm 10\%$.

SUPPLY PROTECTION:

Supply voltage must be limited to 7 V.

MAXIMUM CURRENT CONSUMPTION:

300 mA.

SENSITIVITY:

ERROR SENSITIVITY:

200 ns. Errors greater than this are detected and stretched to at least 0.1 second.

DELAY VARIATION IMMUNITY:

50 ns. Errors shorter than this value are considered spurious and ignored.

TEMPERATURE:

0° to 55°C.

DIMENSIONS:

1.4 in deep, 3.375 in wide, 7.15 in long (3,56 x 8,55 x 18,2 cm).

WEIGHT:

Net, 2 lb 6 oz (1,14 kg). Shipping, 3 lb 6 oz (1,62 kg).

ACCESSORIES INCLUDED:

1 test board; 10 blank reference boards; 1 carrying case.

ACCESSORIES AVAILABLE:

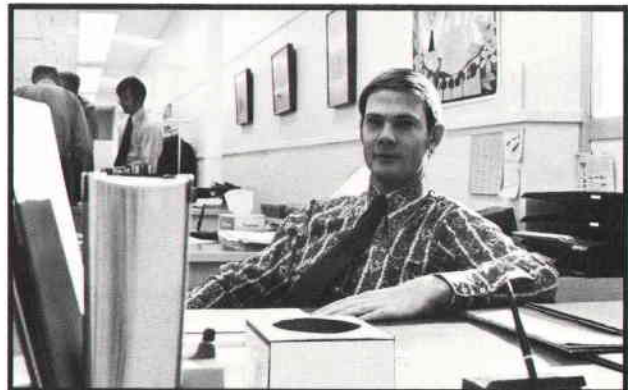
Model 10541A supply of reference boards includes 20 blank reference boards and storage container. Price: \$50.00.

PRICE:

Model 10529A: 1 to 4 units, \$295.00. 5 to 9 units, \$290.00. 10 to 19 units, \$285.00. For larger quantities, please consult Hewlett-Packard.

MANUFACTURING DIVISION: SANTA CLARA DIVISION

5301 Stevens Creek Boulevard
Santa Clara, California 95050



Jesse Pipkin

Five years as a U.S. Air Force navigator taught Jesse Pipkin how to get where he wants to go. So far, that's been to the University of Florida, where he got his B.S.E.E. degree in 1967 and then to HP as an applications engineer specializing in the 8540A Network Analyzer. Coincidentally, among the duties of that job was to be navigator/pilot for a mobile network analyzer demonstration unit. Jesse finally landed at HP's Santa Clara Division, where he's now product manager for logic test devices. He's a member of IEEE and an avid skier.

The Well-Modulated Synthesizer

While preserving synthesizer qualities, means are found to modulate output widely, precisely, and remotely.

By James E. Stinehelfer

FROM THE OUTSET OF THE 8660 SYNTHESIZER PROGRAM it was planned that the system would have a plug-in modulator (Model 86632A) whose capabilities would fully complement its other characteristics. Modulation is not a common feature in synthesizers; much less common are the refinements ultimately incorporated:

- totally programmable modulation in 100 calibrated 1% steps, AM or FM
- low-drift center frequency with FM deviation and rate to 1 MHz
- local source for 400 and 1000 Hz signals
- precise preservation of modulation level despite external source variations
- AM at low rates with minimal phase shift

All of the modulator plug-in's front-panel functions are programmable (Fig. 1). These include MODE (AM or FM, the latter in deviation ranges of full-scale 10 kHz, 100 kHz, and 1 MHz), SOURCE (internal 400 or 1000 Hz, external ac-coupled and leveled or dc-coupled), MODULATION LEVEL, and FM-CF-CAL (automatic center-frequency calibration) of which more, later. The block diagram (Fig 2) describes the internal relations among the functional elements.

Sources

The source of modulation can be internal or external. The internal source is a low-distortion, bridged-tee oscillator supplying 400-Hz or 1000-Hz signals. A portion of the modulating signal is delivered to a front-panel connector to synchronize other test equipment when internal source is selected.

If the external ac-coupled source position is selected, the modulation is first amplified or

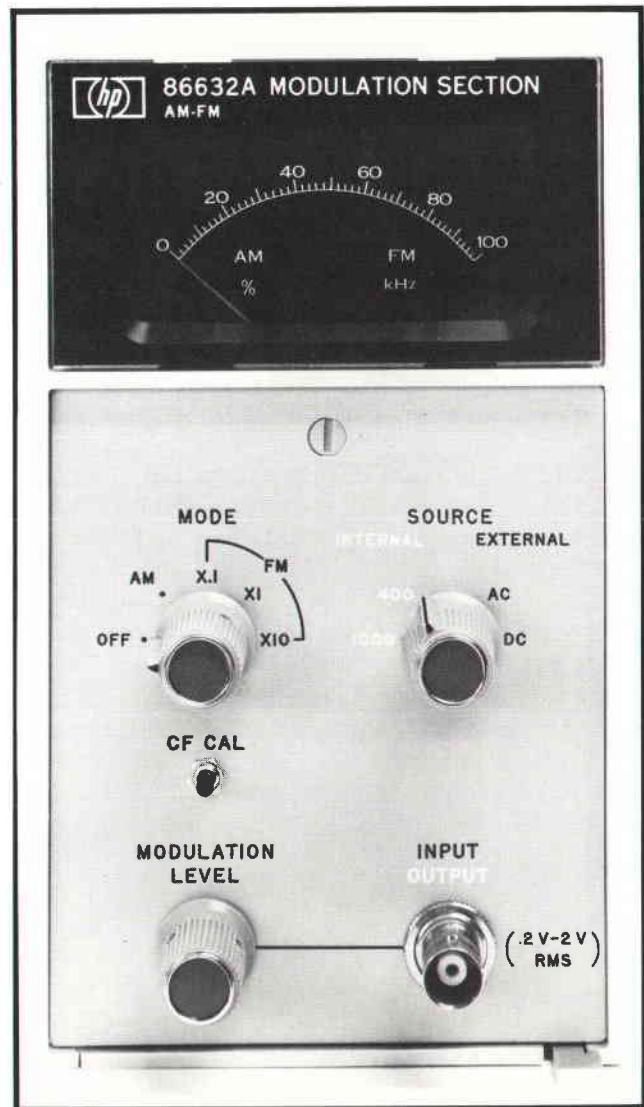


Fig. 1. 86632A front panel.

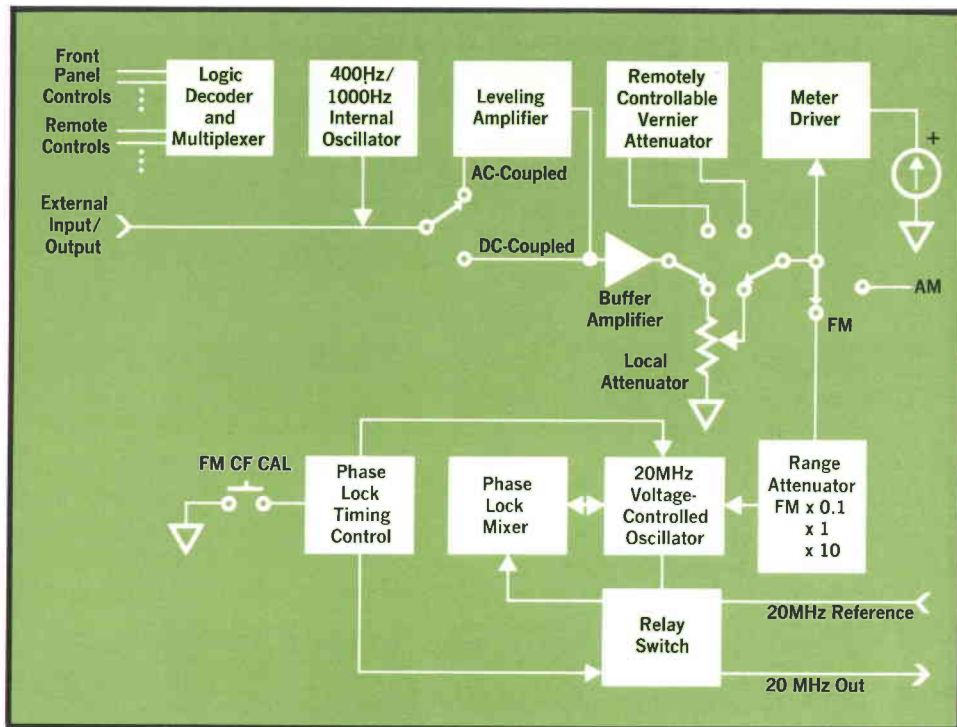


Fig. 2. 86632A block diagram.

attenuated to a level of $1.8 V_{rms}$ by the leveling amplifier. This level of output is maintained even though the signal may vary from 20 Hz to 1.0 MHz and from 0.2 to $2.0 V_{rms}$. With the input signal level thus fixed, the remote-controllable vernier attenuator is calibrated, and hence percent modulation is calibrated at any of the hundred selectable steps. In local control the $1.8 V_{rms}$ signal from the leveling amplifier is supplied to the front-panel vernier, which allows essentially infinite variation of modulation indices.

The leveling amplifier is a fixed-gain, low-distortion amplifier preceded by a variable attenuator. Its output level is detected by a peak-to-peak diode detector and compared to a dc reference. The error signal is amplified, level-shifted, and used to control a photoresistor which is the variable element of the input attenuator. Because of the need to accept low modulation rates, down to 20 Hz, the leveling loop bandwidth must be correspondingly low. As a result the settling time of the leveling amplifier can be several seconds for a large perturbation in input level. This may not be tolerable, as in cases where the instrument is computer-controlled. It may also be necessary to operate below 20 Hz, and in some applications (VHF omni-range equipment, for example) careful preservation of phase relations at very low frequencies can also be required. In such cases a dc mode of operation may be selected, bypassing the leveling amplifier.

Amplitude Modulation

Amplitude modulation is not accomplished within the plug-in, but instead by applying the processed modulating signal to the leveling loop of the RF plug-in, which performs the actual modulation.

Frequency Modulation

In the FM mode the selected source, leveled or unleveled as desired, is fed to a three-state RANGE attenuator. This determines whether 100% modulation shall be calibrated at 10-kHz, 100-kHz, or 1-MHz deviation. Next the signal is applied to the voltage-variable capacitor which tunes a 20-MHz oscillator. The output of this oscillator, now a frequency-modulated signal, is then substituted for the 20-MHz synthesized signal in the RF plug-in, and is directly mixed into the output frequency. The 20-MHz VCO can be modulated up to 1 MHz both in deviation and rate.

'FM CF CAL'

Once the FM mode is selected, the primary output frequency of the RF section is no longer a synthesized signal, i.e., its frequency is no longer phase-coherent with the master crystal oscillator. Its true output frequency is the selected center frequency plus any error in the 20-MHz VCO of the modulator plug-in.

To minimize this effect, an automatic calibration

cycle, FM CF CAL, has been included (Fig. 3) which momentarily interrupts the modulation and phase locks the 20-MHz VCO to a 20-MHz synthesized signal, stores an error correction voltage, and returns to normal operation. This FM Center Frequency Calibration cycle requires approximately five seconds and can be initiated from the front panel or may be programmed through the rear panel remote connector. The frequency error immediately after calibration is typically less than 100 Hz regardless of the center frequency selected on the 8660A.

The 20-MHz VCO

The FM capabilities of the modulation section are primarily determined by the characteristics of the VCO and its bias circuits. A significant part of the engineering accomplishment was obtaining simultaneously the linearity, stability, and sensitivity required. The basic oscillator uses a matched set of three hyperabrupt variable-capacitance diodes to tune a tank circuit over the required range of 19 MHz to 21 MHz. Careful selection of the operating bias voltage allows this excursion with a sensitivity of approximately 1 Hz/ μ V and nonlinearity less than $\pm 2\%$.

The stability of the oscillator is mainly a function of the ability of the 'sample and hold' circuit used in the FM CF CAL cycle to 'hold' the correction voltage. The use of a special capacitor and MOSFET plus a 0.0 volt nominal bias voltage yields a time constant for the circuit on the order of 10^9

seconds. This translates to approximately a 2 Hz/min drift rate. Further through careful temperature compensation, stability with temperature is typically 15 PPM/ $^{\circ}$ C. After ambient temperature stability is reached all temperature-related drift may be removed by the FM CF CAL cycle (Fig. 3).

Mechanical

Often the physical constraints placed on the mechanical design of a plug-in result in severe compromises to ease of assembly, test, and service. The 86632A, however, aims to be an example of lack of compromise on such features. Hand wiring has been minimized through the use of a structural motherboard, a harness board, and a 16-wire ribbon cable with IC-type flat-pack connectors.

Board guides and extractors are color coded to establish position, polarity, and assembly number for each of five plug-in circuit boards. The rear housing, which provides thermal stability and RF shielding for the 20-MHz VCO, relay switch and phase lock mixer, can be pivoted away from the side frames allowing access to all components without major disassembly. Within the rear housing a low-cost RF feedthrough was developed which eliminated three external RF cables and their associated connectors by allowing board-to-board connection through the inside partitions of the housing.

The entire package has sustained shock levels in excess of 200 G's without mechanical or electrical failure.

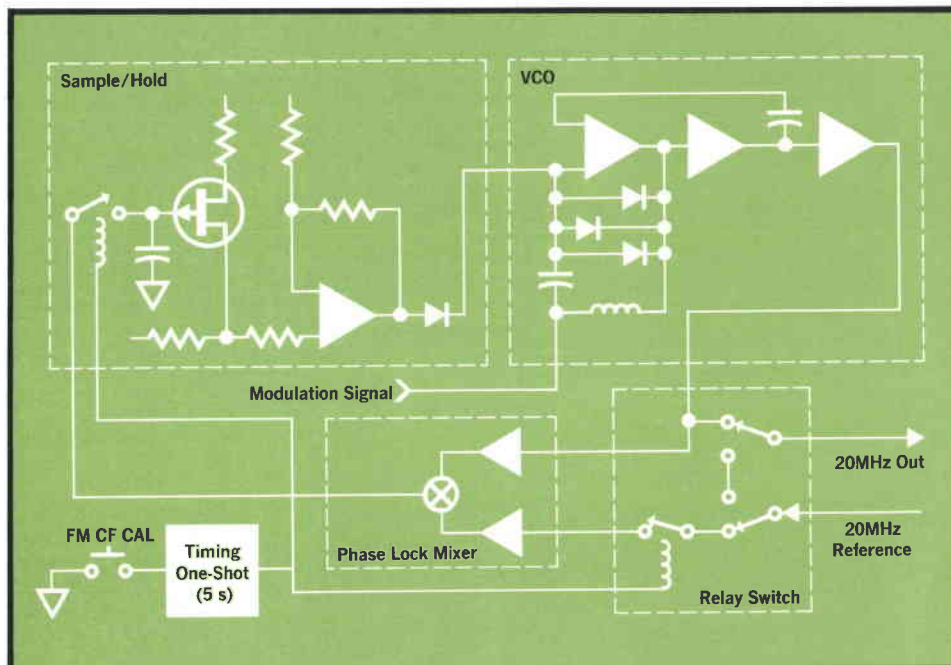



Fig. 3. FM Center Frequency Calibration block diagram.

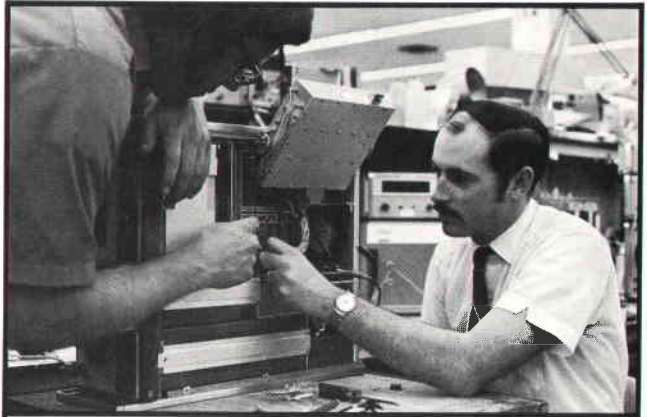
The 86631A Auxiliary Section

The auxiliary section is provided for those with limited modulation needs. It performs all necessary system interconnections and also provides direct access to the RF section level control. Through a front panel BNC connector all AM capabilities of the RF section may be exercised (though remote operation is not possible). The sensitivity of the input is $1 V_{rms}/100\%$ and percent AM is linear with input level over this range. The maximum frequency and modulation depth obtainable is dependent on the RF section installed.

Perhaps one of the primary uses of this plug-in will be as a basic housing for those who wish to build special-purpose modulation sections.

Acknowledgments

The modulation section had been a child of many fathers when I was assigned its development. John Hasen did the preliminary block diagram and also acted as an invaluable consultant throughout the entire project. Art Bloedorn did the initial design of the 20-MHz VCO and several of the 8660A/B oscillators. Bob Gallien and Brad Stribling both contributed design approaches which were eventually used. Jim Fleming did all of the product design and contributed greatly to the entire project. 



James E. Stinehelfer

Jim Stinehelfer came to California 15 years ago, from Michigan. He was a part-time employee at HP even as a Stanford undergraduate, and he became a fulltime engineer soon after taking his BS in EE in 1965.

His duties were successively in charge of environmental testing, then in synthesizer design. Jim went on, under the HP Honors Program, to take an MBA at nearby Santa Clara University, meanwhile marrying and starting a family. He had to give up his Cessna 170 on the arrival of the second youngster, but he still flies, renting a plane now and again for long weekends in places like the Grand Canyon. Most fall weekends you can find Jim in the fields hunting with his Labrador Retriever 'Gypsy.'

SPECIFICATIONS

HP Model 86632A AM/FM Modulation Section

INTERNAL MODULATION

AM:

RATE: 400 Hz and 1 kHz $\pm 5\%$.
DEPTH: 0 to 100% (or maximum specified for RF unit installed).
METER RANGE: 0 to 100%.
METER ACCURACY: $\pm 5\%$ FS.

FM:

RATE: 400 Hz and 1 kHz $\pm 5\%$.
DEVIATION: 0 to 1 MHz peak
(or maximum specified for RF unit installed).
METER: 3 ranges—10 kHz, 100 kHz, 1 MHz.
METER ACCURACY: $\pm 5\%$ FS.

EXTERNAL MODULATION

Input Level Required, ac-coupled mode: 0.2V to 2.0V.
Input Level Required, dc-coupled mode: $1.8V_{rms} \pm 50$ mV.
Input Impedance: 600 Ω .

AM: dc to 1 MHz in dc mode, 20 Hz to 1 MHz ac mode.
Rate, depth, and meter accuracy same as INTERNAL.

FM: Rate dc to 1 MHz in dc mode, 20 Hz to 1 MHz ac mode.
Deviation, meter ranges and accuracy same as INTERNAL.
DISTORTION: Partially determined by distortion of external modulating signal, which must be under 0.3% to meet RF Section distortion specifications, e.g. $<1\%$ @ 30% AM, $<3\%$ @ 70% AM, and $<5\%$ @ 90% AM with 86601A 0.1–110 MHz RF Section.

REMOTE PROGRAMMING

FUNCTIONS: All 86632A front panel controls are programmable through the 8660A or 8660B mainframe programming interface.
Resolution of Remote Modulating Setting: Steps of 1/100 of the range selected.
Accuracy of Remote Modulation Setting: $\pm 5\%$ of setting when using ac or internal sources.

GENERAL

SIZE: Plug-in for 8660A or 8660B mainframe.
WEIGHT: Net, 7 lb (3,2 kg).
POWER: From 8660A or 8660B mainframe.
PRICE: \$900.00.

MANUFACTURING DIVISION: MICROWAVE DIVISION
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