JULY 1978

HEWLETT-PACKARD JOURNAL

An Intelligent Peripheral for Measurement and Control

Communicating with the computer in a high-level language, this new computer front end independently executes analog and digital measurement and control tasks. It has a full complement of input/output interfaces and many built-in service facilities.

by Ray H. Brubaker, Jr.

THE TREND TODAY in computer systems is clearly towards distributing the computing power instead of concentrating it in one large central computer. Examples of this trend are the growing number of networks of small computers and the increasing variety of intelligent computer peripherals and instruments.

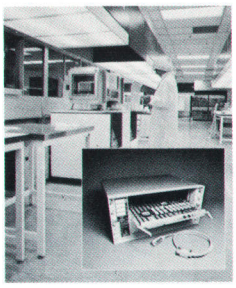
Fig. 1 shows a block diagram of a typical measurement and control system based on the 2240A Measurement and Control Processor. Analog and digital interfaces plug into the 2240A to interface to various sensors, switches, controls, and actuators (see Fig. 2). The processor's communication link to the computer is the Hewlett-Packard Interface Bus, or HP-IB, Hewlett-Packard's implementation of IEEE standard 488-1975 (ANSI standard MC1.1). Careful design of message protocol and data formats makes the 2240A compatible with virtually any computer, calculator, or intelligent terminal that supports the HP-IB.

Using standard HP-IB cables, the 2240A can be located up to 20 metres (65 feet) from the computer or other controller. For remote applications, the HP-IB can be brought to the 2240A by any of a variety of multidrop, point-to-point, or telephone line interfaces. For example, an HP 3070B Terminal (see article, page 19) can be used as a parallel-to-serial interface to a twin-conductor cable system that allows 2240As to be located up to 2 km (1.2 miles) from a computer. The 3070B can also interface the 2240A to a computer that does not support the HP-IB.

High-Level Measurement and Control Language

The 2240A understands a language of simple two-character commands called the Hewlett-Packard Measurement and Control Language, or HP-MCL.

Efficiency and reliability are the goals of distributed processing, and one means of reaching these goals is specialization. A computer or instrument designed for and dedicated to one job is more efficient



Cover: *Model 2240A Measurement and Control Processor (inset) is designed to interface a computer to real-world sensors and controls. An example of a laboratory automation application for the 2240A is computer control of the metal-sputtering system shown here. Hoped-for benefits are better repeatability and less need for operator attention. Other 2240A applications are equipment control, product testing, process control, energy management, and facility monitoring.*

In this Issue:

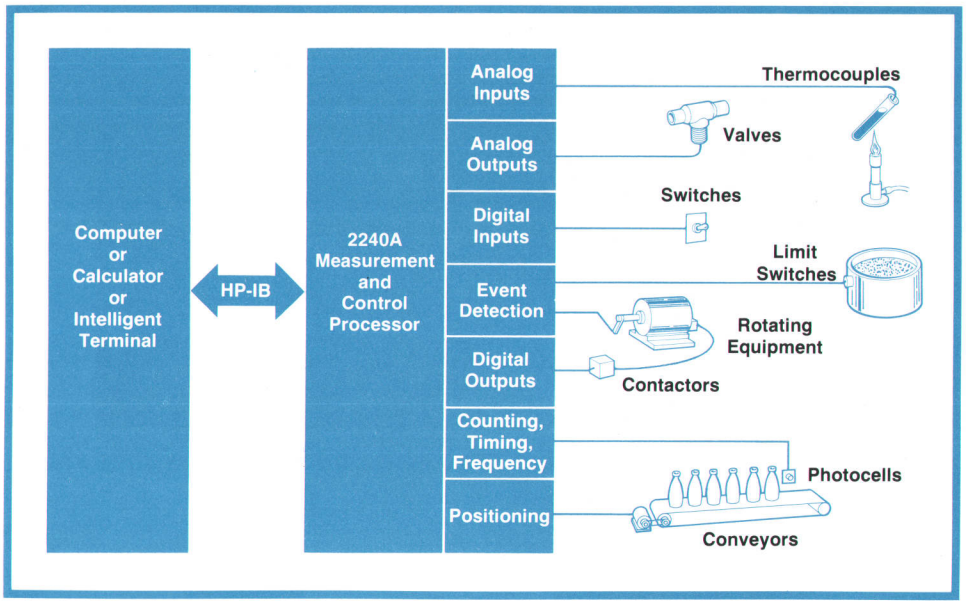


Fig. 1. *A general measurement and control system consisting of the 2240A Measurement and Control Processor linked to a digital computer by the HP interface bus and to appropriate sensors and actuators by plug-in analog and digital function cards. The sensors, actuators, and function cards vary with the application.*

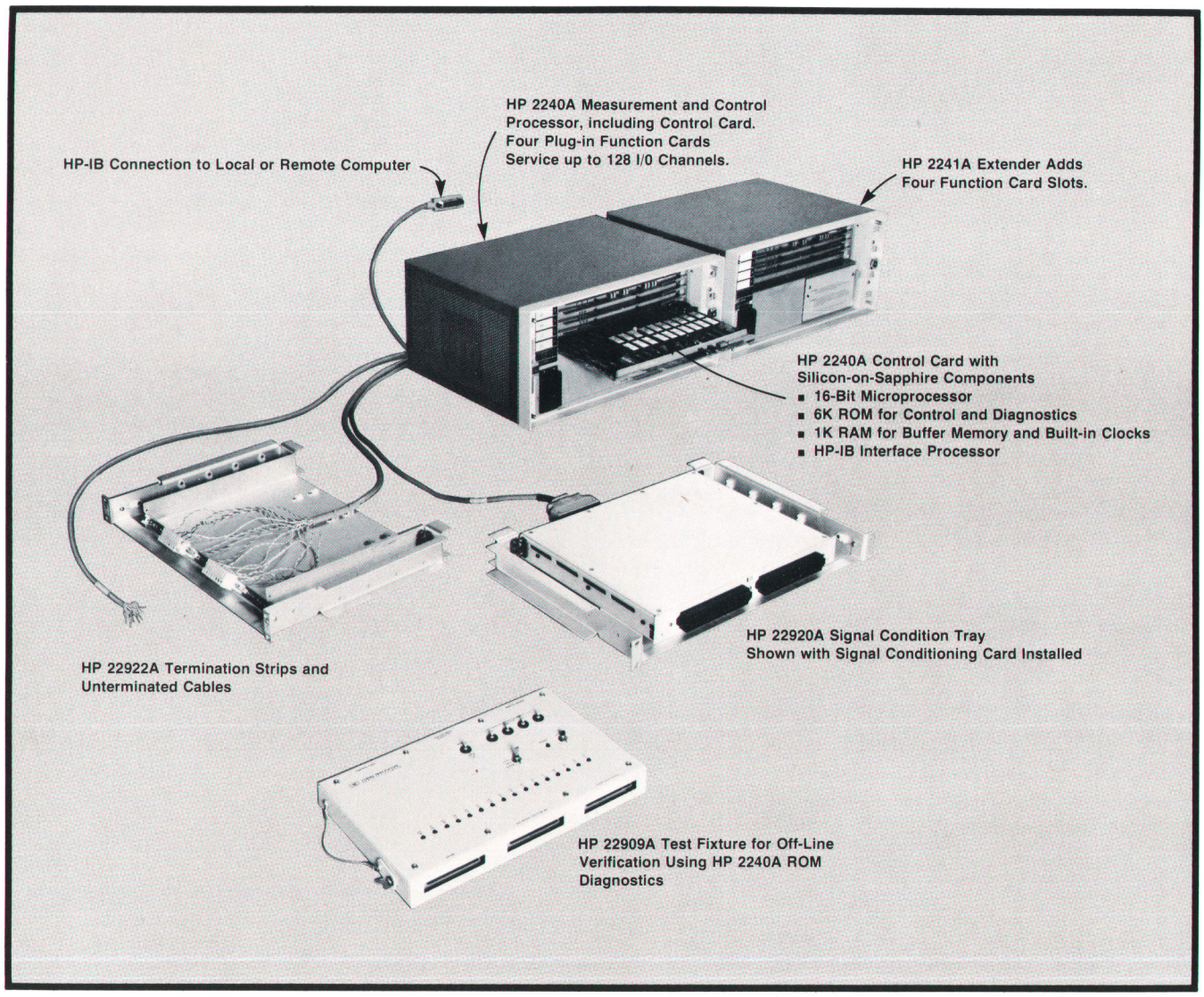


Fig. 2. *Components of the 2240A Measurement and Control Processor System.*

HP-MCL Commands

	Digital Input		**Counter-Stepper**
FI	Field Input	RC	Read Count
DI	Digital Input	ST	Start Totalize
		SF	Start Frequency or Period
	Digital Output	SS	Start Stepper
FO	Field Output	CR	Counter Reset
DO	Digital Output	CT	Counter Test
	Common Interrupt		**Timing And Sync**
MI	Mask Register Input	WB	Wait before Each Data Transfer
MO	Mask Register Output	WN	Wait Now
SI	Sense Register Input	WT	Wait for Trigger
SO	Sense/Mask Register Output	TP	Timer Preset
		WU	Wait until Elapsed Time
	Analog Input	TE	Read Time Elapsed
AI	Analog Input	TI	Time Interval
RI	Repeated Analog Input		**Supervisory**
AU	Analog Uncorrected Input	IC	Interrupt on Completion
RU	Repeated Uncorrected Analog Input	IN	Interrupt Now
AC	Analog Calibrate	PM	Processor Mask
AE	Analog Autocalibration Enable	SM	Set Require Service Mask
AD	Analog Autocalibration Disable	SN	System Normalize
		BK	Block Current Result
		BD	Block Default
		RP	Repeat
	Analog Output	NX	Next
AO	Analog Unipolar Output		
AB	Analog Bipolar Output		**Test**
RO	Repeated Analog Unipolar Output	VE	Verification Echo
RB	Repeated Analog Bipolar Output	SC	System Configuration
		OT	Offline Test
			Primitive
		SR	Sequential Read
		RR	Repeated Read
		SW	Sequential Write
		RW	Repeated Write

Fig. 3. *The 2240A is controlled by sending commands over the HP-IB in a high-level language called the Hewlett-Packard Measurement and Control Language. HP-MCL includes 48 commands for input/output, timing, synchronization, and supervision. Commands may be used together to form simple programs called requests.*

than one of general design or one that addresses several unrelated tasks at once. Recent examples of specialized, intelligent devices are the HP 2648A autoplotting graphics terminal[1] and the HP 9872A four-color plotter.[2] Microprocessors are the key elements in the functional specialization of this equipment.

A fast new 16-bit silicon-on-sapphire (SOS) microprocessor[3] has made possible a new specialized peripheral that interfaces a computer to real-world sensors and controls. The HP 2240A Measurement and Control Processor is the first product to use HP's silicon-on-sapphire technology, and the first product of its kind in the industry. It is designed for applications such as equipment control, product testing, laboratory automation, energy management, and facility monitoring. Connected to the application through analog and digital interfaces, the 2240A performs assigned tasks quickly and independently, functionally separate from the controlling computer. Using a high-level command language, the computer can delegate a complete task to the 2240A. The computer can then return to what it does best—computing—and leave the peripheral to do what it does best, which is measurement, control, and synchronization of the outside world of machines and experiments. Self testing, diagnostics, and error reporting are built into the 2240A. These features combine to simplify and expedite the design, programming, debugging, and long-term maintenance of an automated application.

HP-MCL is designed to describe measurement and control operations synchronized with the timing and motion of the user's equipment or process. Fig. 3 lists the 48 commands that make up the language. A typical command is AI, analog input, which is used for making voltage or current measurements from variable output sensors such as thermocouples and potentiometers. The command AI,2,1,10 instructs the 2240A to take measurements from the analog card in slot 2, starting with channel 1 and continuing for ten channels.

While HP-MCL is easy to learn and use, its power lies in the ability to string together any sequence of commands to describe a complete task to be performed. Such a measurement and control task is called a request, and any measurements taken during its execution form a result. Fig. 4 shows a typical request and its result. The commands cause the 2240A to make a series of measurements and actuate a control when an event is detected. An example of such an event is the tripping of a photocell as a shaft

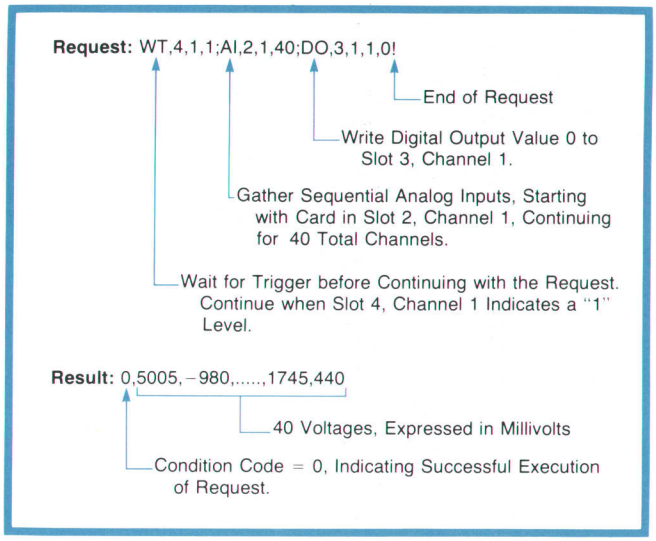
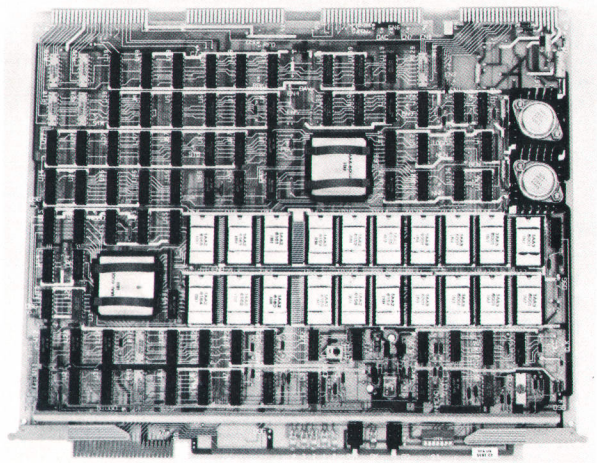


Fig. 4. *The 2240A receives requests from the computer as sequences of HP-MCL commands describing measurement and control operations to be performed. Results, consisting of measured data, timing information, and a condition code, are returned to the computer.*

First HP Product to Use Silicon-on-Sapphire Technology

The 2240A Measurement and Control Processor is the first product to incorporate HP's CMOS* silicon-on-sapphire (SOS) microprocessor family.[1] Microsecond instruction times, 16-bit architecture, and optimization for controller applications are key features of this family. The 2240A takes advantage of the speed of SOS to provide high-level language programming while preserving real-time response. 12-volt CMOS logic is used throughout the 2240A for noise immunity and low power consumption. This logic level is directly compatible with the SOS chip family.



Shown here is the 2240A's control card, which includes 22 SOS components. The 16-bit MC² microprocessor is used, along with 12K bytes of read-only memory (ROM), 2K bytes of random-access read-write memory (RAM), and the PHI processor/HP-IB interface. The memory cycle time is 100 nanoseconds, compatible with the cycle time of the microprocessor, and the I/O handshake lines of the PHI chip couple directly to those of the MC² chip.

Characteristics of the SOS chip family are as follows:

MC²: 16-Bit Microprocessor
- Single-chip 16-bit static microcontroller
- 16-bit add in less than one microsecond
- Seventeen internal registers
- Direct interface to mixed-speed memory and I/O
- 300 mW power consumption
- 11,000 transistors in 36 mm².

8K-Bit ROM
- 1024 bytes × 8 bits
- 100 ns maximum access time
- 75 mW power consumption
- 15,000 devices in 18 mm².

2K-Bit RAM
- 256 bytes × 8 bits
- 100 ns maximum access time
- 75 mW power consumption
- 15,000 transistors in 20 mm².

PHI: HP-IB Interface
- Complete HP-IB (IEEE 488-1975, ANSI MC 1.1) interface to 8-bit or 16-bit microprocessor
- Data rate to 1 Mbyte per second
- DMA transfer capability
- Compatible with CMOS or TTL
- 350 mW power consumption
- 9000 transistors in 30 mm².

*CMOS = complementary metal-oxide-semiconductor.

Reference

1. B.E. Forbes, "Silicon-on-Sapphire Technology Produces High-Speed Single-Chip Processor," Hewlett-Packard Journal, April 1977.

rotates. The result contains a condition code and the requested measurements.

Since the entire request is copied into a buffer within the 2240A, the commands can be executed at a speed commensurate with the application. This is generally much faster than would be possible if the computer had to interact on a command-by-command basis.

The structure of the language is compatible with the communications mechanisms available in most computer programming languages. Simple read, write, and print statements are used to transfer requests and results between the computer and the 2240A. Sending a request to a 2240A is no different from printing the same message on a line printer. No special subroutines, I/O routines, or drivers are needed. Fig. 5 shows programs in three different languages for two different computers performing the same measurement operations.

Keeping up with the Real World

"Real time" for a computer system can be defined in many ways, but in the measurement and control field, its meaning is clear: the computer system must keep up with the physical motion and timing of the equipment being tested or measured or controlled. The timing constraints of a real-time application are usually very easy to describe. Typically, certain measurements must be made at specific intervals or controls must be actuated within a certain period following a triggering signal. It can be complicated, however, to determine whether a computer can keep up with the prescribed rates. This depends upon the efficiency of the computer's operating system and on competition from other programs, as well as on the raw speed of the processor. With several difficult-to-predict variables involved, less-than-convincing benchmarks must often be used.

The measurement and control processor solves this

problem for many applications by allowing the customer to partition a problem into a computational part and a real-time part. Any computer that meets the computational needs may be used. The 2240A handles the real-time part and makes measurements and actuates controls as necessary. The 2240A is optimized for this job, and its capabilities are straightforward and predictable. In analyzing a typical application, a request can be composed using the measurement and control language, and its timing can be determined by adding the times listed in the manual for each command. Usually this makes it obvious whether the 2240A will work or not. Fig. 6 presents an example where the 2240A's timing meets the requirements of the application. Note that there is no mention here of the type of computer, its performance, or the speed of the communication link connecting it to the 2240A. These factors are not relevant to the basic will-work/won't-work decision. This is characteristic of many product-testing and data acquisition applications.

In other situations, the computer is in the loop. In other words, the computer is required to perform computations on an ongoing basis. This is characteristic of closed-loop control applications. Fig. 7 describes a laboratory experiment automated by the 2240A. It shows the 2240A repeatedly taking measurements and updating control positions. The 2240A keeps track of the time and starts each new scan. In this case, the performance of the computer is important, but only in that it must not use more than 40.2 milliseconds to compute new control values. The exact time used in computation is not important.

Decoupling computation from measurement and control timing constraints, as illustrated by these examples, is a major contribution of the 2240A Measurement and Control Processor.

FORTRAN IV (HP System 1000)

```
      DIMENSION VOLTS (40)
      WRITE (16,100)
  100 FORMAT ("WT,4,1,1;AI,2,1,40;DO,3,1,1,0!")
      READ (16,*)CODE,(VOLTS(I),I=1,40)
```

BASIC (HP System 1000)

```
10 DIM V (40)
20 PRINT #16;"BK,1;WT,4,1,1;AI,2,1,40;DO,3,1,1,0!"
30 READ #16;C
40 FOR I=1 TO 40
50 READ #16;V(I)
60 NEXT I
```

HPL (HP 9825A Desktop Computer)

```
0: dim V[40]
1: wrt 701,"WT,4,1,1;AI,2,1,40;DO,3,1,1,0!"
2: red 701,C
3: for I=1 to 40
4: red 701, V[I]
5: next I
```

Fig. 5. *Requests and results are programmed using the standard read, write, and print statements of most computer languages. Here are programs in three different languages for two different computers that cause the same measurement operations to occur.*

Simplified Maintenance and Support

Any real measurement and control application must be maintained and supported after initial development and checkout. This includes upgrading hardware and software to incorporate new features as well as troubleshooting failed components. Distributing intelligence to the 2240A helps in both of these areas.

Separating timing from computation makes 2240A-based real-time applications less sensitive to changes in computer performance. A different computer may be installed at some future date without affecting the timing of a critical control loop. Simi-

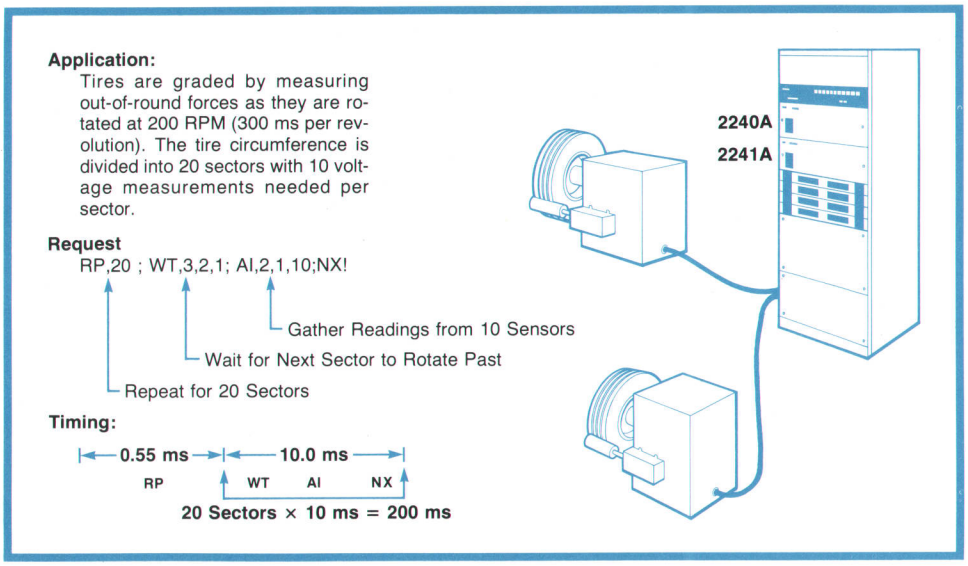


Fig. 6. *By adding the execution times given in the 2240A manual for each instruction, a quick determination can be made as to whether or not the 2240A will do the job, with no need for benchmarking. In this typical application, the 2240A can complete the required measurements in 200 ms, 100 ms less than the allowable time.*

Measurement and Control Processor Monitors HP Facility

by Robert B. Grady

At HP's Sunnyvale, California plant, where the 2240A Measurement and Control Processor was developed, facility engineers had begun to centralize the monitoring and control of the building's machinery and parameters long before the 2240A project. Once the project was under way, it was a natural idea to automate this monitoring and control using a prototype 2240A and an HP 9825A Desktop Computer as a controller. The application served as an excellent test site for the 2240A and the variety of analog and digital function cards developed for this product line.

Timing Considerations

The facility monitoring system is based on time of day and elapsed time. The 2240A has both of these real-time clock capabilities, so no external clocks or time bases are necessary. The software system is based on easy-to-modify tables. For example, one table contains measurement time intervals. For each entry in this table, another table contains a list of measurement points to be sampled at the specified interval. The 2240A command TI (time interval interrupt preset) is given after each measurement sequence to establish the next time interval, and after the specified time elapses, the 2240A generates an interrupt to the controller to initiate the acquisition of data. A simple example of this operation is the on/off digital input points, which are examined once every 15 seconds, generating listings of the type shown here:

```
ON/OFF STAT PTS
- - - - - - - -
NAME OF PT
. . . . . . . .
CHAN/ON TIME/%ON
A/C 1
097  0444.1  100
CBP 1
098  0387.3   87
```

This excerpt shows that chiller boost pump #1 (CBP 1) is monitored by channel 98 and has been active 87% of the time, or 387.3 minutes.

Concurrently, the time-of-day timer in the 2240A displays the time of day and determines when facility reports are due (at 0600 and 1800 each day).

Control-Panel Functions

The 2240A is particularly convenient as a simple means of providing the operator interfaces needed in any system. A pushbutton switch mounted above the 2240A can be connected either to a common interrupt card or to a counter-stepper card to provide an interrupt to the controller. When the switch is actuated the operator has the options shown below.

```
SUPER INTERRUPT

0 RESUME
1 FACILITY RPT
2 MONITOR A CHAN
3 CHANGE TIME
4 CHNG TIME TBL
5 CHG PK PWR LMT
```

The 2240A can also turn on an alarm to alert personnel to dangerous conditions. With a 2240A and a controller, a wide variety of conditions can be examined for alarm generation.

Monitoring Electrical Peak Power

Probably the most significant single parameter in the facility is peak power. The cost of commercial electrical energy is based on both the amount of electricity consumed and the highest peak rate of consumption during some predetermined time interval. For the HP Sunnyvale facility, this time interval is one-half hour.

A counter-stepper card counts pulses that represent electrical use, and a running record of the latest thirty minutes of readings is maintained. Whenever a projection of the most recent ten minutes exceeds an established limit, an alarm is generated and personnel have twenty minutes to correct the temporary excessive use. A typical alarm message is shown below:

```
01:35:01 PM
Projected Pk Pwr
          1355
**ALARM**
```

Although not presently done, it would be easy for peak power consumption to be automatically controlled in graduated steps, first by a printout showing shut-down priorities, and ultimately by automatic control of the shut-down and start-up sequences.

When the daily reports are generated, electricity consumption is summarized as shown here:

```
ELECTRICITY USE
- - - - - - - -
Projected Month
    0144730 Kwh
Peak Hour/Target
    0000997 Kwh
    0001200 Kwh
```

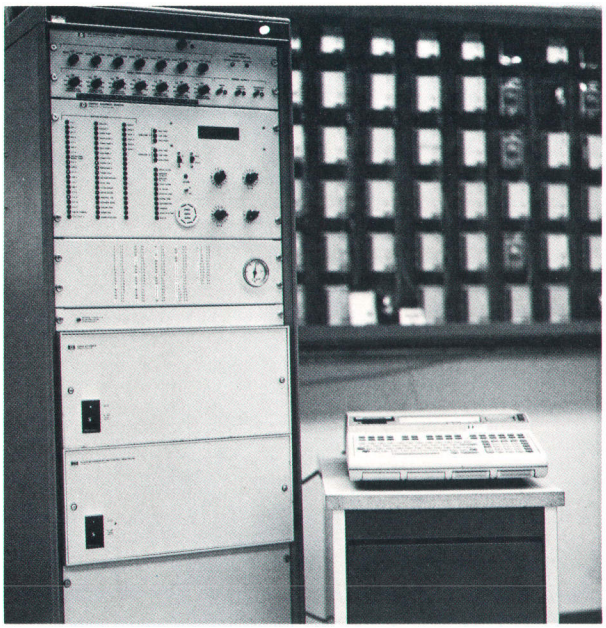
Solar Heating

The Sunnyvale facility first installed supplementary solar heating in 1973. There are now 448 panels in the system, and these provide an average of seven million BTUs of energy daily. Two channels of an analog input card are used to monitor temperature points in the solar heating system. Since flow rates are known, the number of BTUs generated during the day is easily determined. Shown here is a typical printout giving the results of such a computation.

```
SOLAR HEATING
- - - - - - -
Btu's Collected
        9519723
Max Btu Rate/Hr
        1499042
Approx $ Savings
              48
```

The internal timing capability of the 2240A helps deal with the high 60-Hz noise levels normally present in such an environment. By taking readings precisely timed over one cycle (repetitive analog input, 17 readings) and averaging them, 60-Hz noise is largely eliminated.

(continued)



Summary

This application is typical of many for which the 2240A provides an excellent solution. It uses both modes of the accurate internal timer to control when events are to occur, and it uses a variety of analog and digital capabilities. There are currently 48 digital on/off points, 16 digital interrupt points, three counter-stepper points, and 74 analog input points in the system. There have been no failures in the 2240A, the 2241A Processor Extender, or the function cards since operation began in May, 1977.

An important benefit demonstrated in this application is the ease with which the system can be upgraded to meet additional requirements. The table structure of the software is easy to change and additional measurement and control functions are easy to add. Since the timing is controlled within the 2240A, even changing the controller from a HP 9825A to an HP 1000 Computer System will be easy when the additional computing power is necessary.

Robert B. Grady

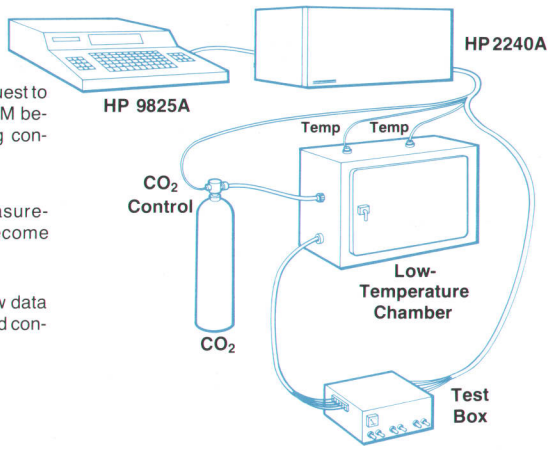
Bob Grady is remote measurement and control project manager at HP's Data Systems Division. Most recently he was project manager for the HP 2240A hardware. He has managed development of the HP ATLAS Compiler, of instrument calibration programs, and of self-test programs for avionics systems. A native of Chicago, Illinois, Bob received his BSEE degree from Massachusetts Institute of Technology in 1965 and his MSEE degree from Stanford University in 1969. He and his wife, who works for HP as a programmer, have a son and live in Los Altos, California. Bob plays basketball and softball in local city recreation leagues and enjoys mountain vacations—hiking, camping or skiing. Recently he equipped his home with a supplementary solar heating system based on the techniques used at HP in Sunnyvale.

larly, enhancements to the operating system or new tasks added to the computer's workload may change program execution times without disturbing overall performance.

For troubleshooting, the 2240A has built-in self-test and verification procedures. Self-test runs without assistance and checks the general health of the 2240A. Verification routines interact with a techni-

Partial Program:

```
Loop: wrt 701,"WU",S,M,"AI,2,1,5;
      AO,4,1,1",V,"DO,1,2,2",W,X,"!"
        (The 2240 is sent an HP-MCL request to
        wait until (WU) the time in S and M be-
        fore gathering data and updating con-
        trols.)
      red 701,C,T[1],T[2],T[3],A,B
        (Condition code and five measure-
        ments are read when they become
        available.)
      cll "Update"
        (Call a subroutine to save the new data
        and compute next time internal and con-
        trol positions.)
      gto "Loop"
        (Cycle complete, repeat it.)
```



Timing:

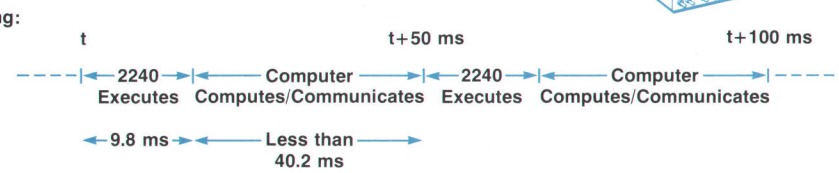


Fig. 7. *In this laboratory automation application, a mechanism is being tested at varying temperatures using a user-designed test box. The 2240A Measurement and Control Processor gathers data at 50-ms intervals and sends it to the 9825A Desktop Computer for processing. Since the 2240A takes 9.8 ms in this application, the computer has up to 40.2 ms to process the data. The exact computation time is not important.*

cian to locate a failing printed circuit card, or to show proper operation for initial customer acceptance. Built-in service tools are a benefit to HP as well as to the customer. For HP they mean that diagnostic tools need not be developed and supported for each computer that might be used with the 2240A. The user benefits since the 2240A can be serviced while disconnected from the computer. Other computer functions can continue undisturbed, and the servicing can be done at the application site, often remote from the computer.

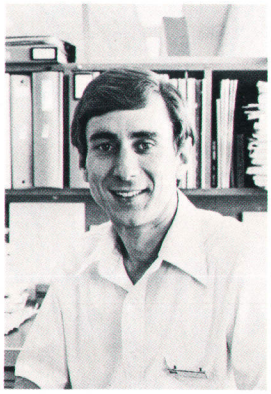
Acknowledgments

Thanks are due many people on completion of a product of this scope. Bill Ray, measurement and control lab manager, refined product objectives and led us to a timely introduction. Pete Palm, Norm Galassi, and Ron Carelli provided marketing inputs. Dick Toepfer provided early project leadership and established manufacturing capability for the 2240A.

Analog function cards were designed by Vince Dauciunas and Dick Cook, who also developed the power supply and breadboard card. Digital functions were the product of Jim Wrenn, Vince Cavanna, and Dave Grus. Jim Wrenn, as number one critic of design, testing methods, and documentation, deserves major credit for product quality. Brice Clark led the signal conditioning effort with Dick Van Brunt and Charlie Martin providing the engineering. Product design was by Dick Riley.

References

1. P.D. Dickinson, "Versatile Low-Cost Graphics Terminal Is Designed for Ease of Use," Hewlett-Packard Journal, January 1978.
2. L.G. Brunetti, "A New Family of Intelligent Multi-Color X-Y Plotters," Hewlett-Packard Journal, September 1977.
3. B.E. Forbes, "Silicon-on-Sapphire Technology Produces High-Speed Single-Chip Processor," Hewlett-Packard Journal, April 1977.



Ray H. Brubaker, Jr.

Native Californian Ray Brubaker obtained BSE and MSCS degrees in 1971 from the University of California at Los Angeles. Graduating with three years of systems programming experience at the UCLA Computer Center, he spent the next few years at the Naval Postgraduate School in Monterey, California as an assistant professor of computer science. He taught a variety of courses and supervised several microprocessor-based research projects. Joining HP in 1974, he helped develop the RTE-III operating system before joining the 2240A team. As project manager for controllers, Ray contributed to management and design of the 2240A's SOS-based control card and HP-MCL firmware. Church activities, carpentry, sports, and flying are a few of Ray's special interests. He and his wife and their two-year-old daughter also enjoy weekend outings in the camper they built.

SPECIFICATIONS

HP 2240A Measurement and Control Processor

MAINFRAME CAPACITY: 4 slots for any mix of function cards listed below; up to 128 analog/digital I/O channels.

HP 2241A EXTENDER: 4 additional slots for function cards; under control of HP 2240A for a total of 256 analog/digital I/O points.

HP 2240A & HP 2241A DIMENSIONS: 482 mm W × 223 mm H × 356 mm D (19 × 8¾ × 14 in.).

WEIGHT: HP 2240A: 13.8 kg (30.4 lb) not including function cards.
HP 2241A: 13.1 kg (28.8 lb) not including function cards.

POWER: 120, 240 Vac; +6%, −28%; 48-66 Hz; 130 watts maximum (including function cards).

ENVIRONMENTAL: 0° to 55°C 2240A air intake ambient.

SAFETY: UL listed under Process Control Standard 1092, Data Processing Equipment (UL478), Office Appliances (UL114).

INTERFACE: HP-IB(IEEE Standard 488-1975); needs controller with ability to handle 5 HP-IB messages (Data, Require Service, Status Byte, Clear, Abort).

PROGRAMMING INTERFACE: Commands to the 2240A and data returned is via standard HP-IB messages. Any HP-IB controller that can send and receive ASCII HP-IB data messages can control the 2240A. Examples are HP 1000, 9825, 9815, and 9830. The HP 2240A receives, interprets, and executes 48 ASCII commands (see p. 4 for complete list) for such tasks as scanning, timing, pacing, and synchronizing with external events.

FUNCTION CARDS (Process/Machine Interfaces)

HP 22900A ANALOG INPUT CARD: 12-bit, ±10V, 20-kHz ADC with 32 single-ended or 16 differential channel input multiplexer. Accuracy with auto correction for gain and drift, .05% input channel span ±1/2 LSB; 0-55°C.

HP 22901A ANALOG OUTPUT CARD: 4-channel, 10-bit, 0-10V (unipolar) or −10V to +10V bipolar DAC outputs (5mA), accuracy ±0.1% @ 25°C, resolution 10mV (unipolar) or 20mV (bipolar).

HP 22901B ANALOG OUTPUT CARD: 4-channel, 12-bit, 0-10V (unipolar), −10 to 10V (bipolar), or 4-20mA (current) DAC outputs, accuracy ±0.025% (voltage), ±0.1% (current), resolution 2.5mV (unipolar), 5mV (bipolar), or 5 μA (current), Kelvin connections.

HP 22902A DIGITAL INPUT CARD: 32-channel TTL/CMOS compatible input levels. Voltage or dry contact sense.

HP 22903A COMMON INTERRUPT CARD: 16-channel TTL/CMOS level compatible (individual channels maskable and transition direction programmable). Voltage or dry contact sense.

HP 22904A DIGITAL OUTPUT CARD: 32-channel, open-collector NPN switch outputs, levels or pulses.

HP 22905A COUNTER/STEPPER CARD: 4 channels individually configurable for frequency or period measurement, event counting or stepper output. TTL compatible.

SIGNAL CONDITIONING CARDS (mount in 22920A tray and Condition Signals—in and out—for Function Cards).

HP 22915A LOW-LEVEL ANALOG INPUT: 16 low-level differential inputs, jumper-selectable gains ±20mV, ±50mV, ±100mV, ±0.5V, ±10V; pads for filters, current loop and open thermocouple detection resistors. 16 amplifier-per-channel outputs connect to 16 single-ended input channels of HP 22900A.

HP 22912A RELAY OUTPUT: 16 Form-C (SPDT) relays, 2A, 125Vac/dc, 60VA.

HP 22913A ISOLATED DIGITAL INPUT: 16 optically isolated and fused channels, user-selected ranges 5-120 Vdc, 16-230 Vac for each channel.

HP 22914A GENERAL PURPOSE BREADBOARD: Layout optimized for 16 analog or digital signal conditioning circuits.

HP 22920A SIGNAL CONDITIONING TRAY (1¾ in. H × 19 in. W × 14 in. D): including 2 Buchanon 28-screw termination connectors for field wiring.

PRICES IN U.S.A.: HP 2240A Measurement and Control Processor, $2750. Installation/Function Test requires HP 22909A Text Fixture ($440). HP 2241A Extender, $1500. Bench Top Covers for HP 2240A/HP 2241A, $60. Function Cards: 22900A, $1600. 22901A, $900. 22901B, $1200. 22902A, $310. 22903A, $450. 22904A, $480. 22905A, $800. Signal Conditioning Cards: 22915A, $1250. 22912A, $290. 22913A, $430. 22914A, $130. 22920A, $165.

MANUFACTURING DIVISION: DATA SYSTEMS DIVISION
11000 Wolfe Road
Cupertino, California 95014 U.S.A.

Firmware Intelligence for Measurement and Control Processing

The HP 2240A demonstrates how HP-IB communications are maturing as instruments gain in sophistication.

by Donald E. Klaiss

MICROPROCESSOR INTELLIGENCE makes it possible to design a new level of capability into today's instruments, so that more of the processing responsibility can be transferred from system computers to the instrumentation. This new breed of peripherals is more powerful, more broadly compatible, and easier to use than any previously available equipment.[1]

Microprocessors execute programs stored in ROM (read-only memory). These programs, or firmware, provide the "personality" of any given microprocessor-based product.

In the HP 2240A Measurement and Control Processor, all activity is controlled by HP's new MC² SOS (silicon-on-sapphire) microprocessor.[2] The microprocessor resides on the 2240A control card (see Fig. 1), and executes firmware programs stored in 12K bytes of on-board ROM. The control card also contains 2K bytes of RAM (random-access-memory) for temporary data storage, the PHI processor/HP-IB interface chip, and interface circuits to manage the measurement and control function cards.

The 2240A communicates with a computer using request and result messages as described in the preceding article. Firmware directs the MC² to receive an incoming request from the PHI HP-IB interface chip and store it in the request/result buffer, which is part of the control card RAM. A request contains one or more commands, such as AI for analog input or DO for digital output. After receipt of a complete request, the 2240A interprets each of the commands in sequence and conveys the appropriate control information to the measurement and control cards. As the request is executed, the microprocessor builds up a result containing a condition code and any desired measurement data. Measured data from external signals is scaled and formatted before it is stored in the result buffer. Analog input readings are corrected for temp-

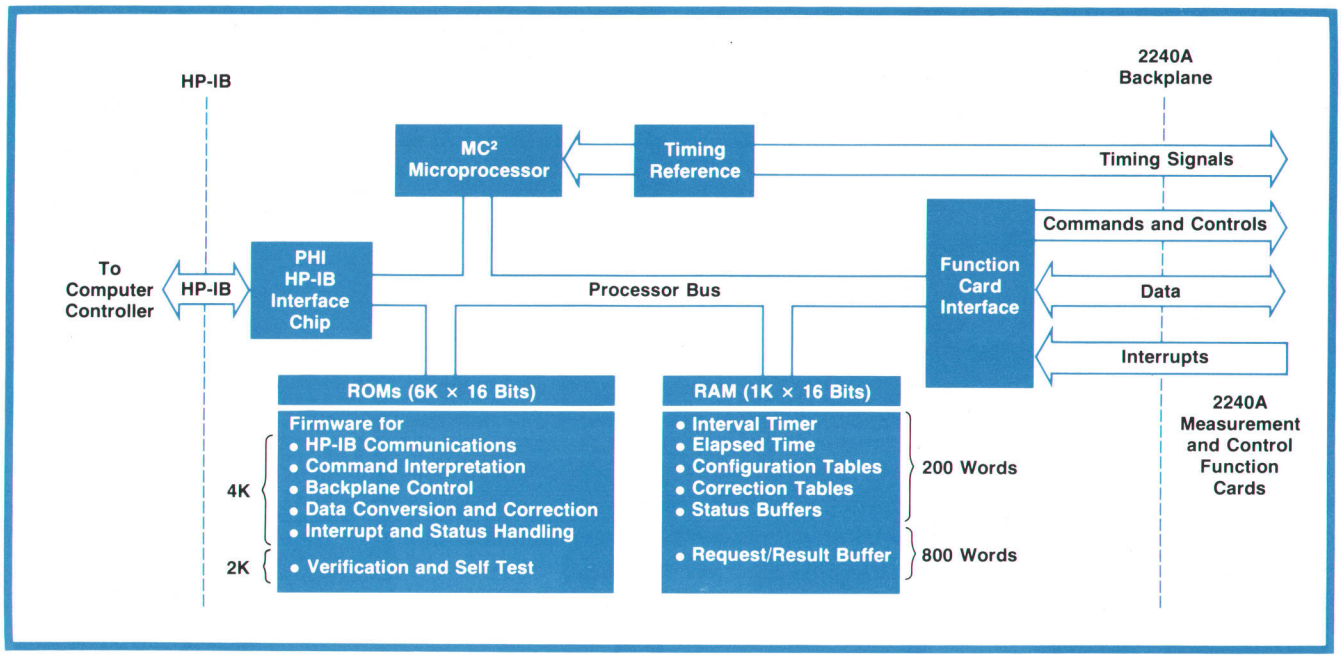


Fig. 1. *On the control card in the HP 2240A Measurement and Control Processor are the MC² microprocessor, the PHI HP-IB interface chip, 2K bytes of random-access memory (RAM), and 12K bytes of read-only memory (ROM). All of these devices are products of HP's silicon-on-sapphire (SOS) technology.*

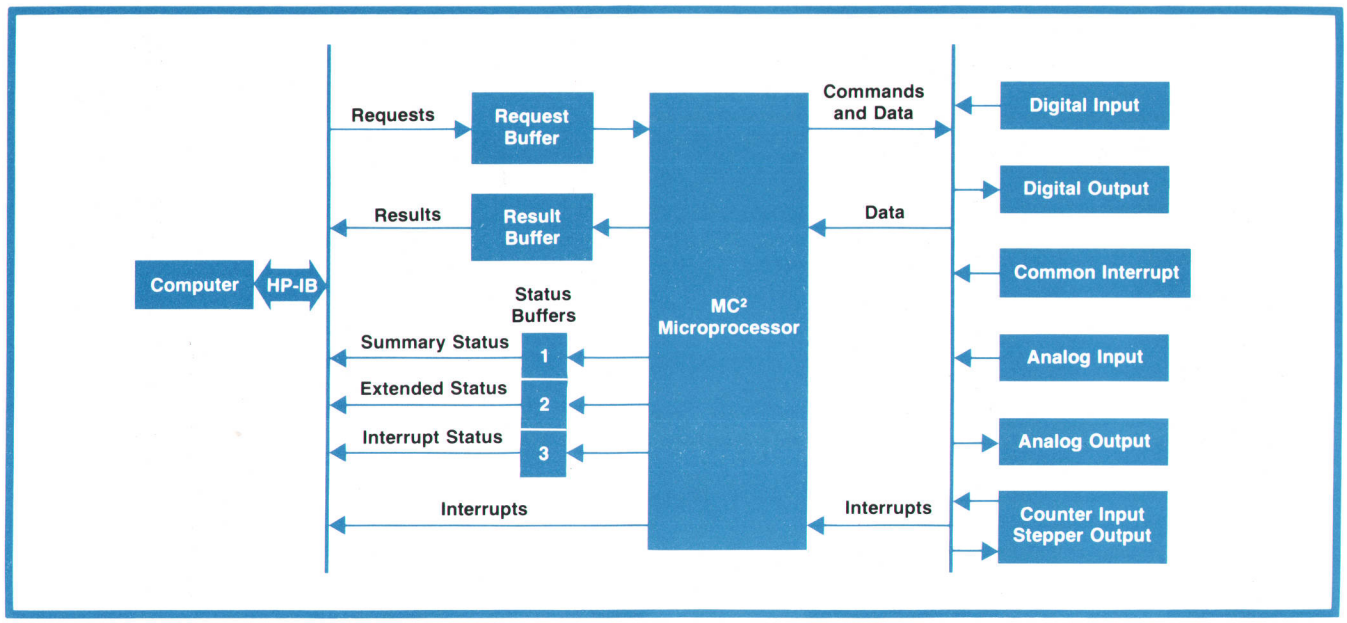


Fig. 2. *The 2240A receives requests from the system computer over the HP-IB, then performs the requested tasks, and returns the results to the computer. Five 2240A buffers are accessible to the computer. The request/result buffers handle normal communications and the other three buffers contain status information.*

erature drift (see box, page 13). When the entire request has been executed, the result is made available for transmission to the computer. A model of this interaction is shown in Fig. 2.

Approximately 1600 bytes of RAM are available for request and result buffering. In addition to the request/result buffer, the 2240A continuously maintains three special status buffers that contain information about the state of the processor. This includes any interrupts that have occurred, the number of the command currently being executed, and detailed information about errors. The status buffers may be read at any time, even interrupting the transmission of a request or a result, without loss of data. Status is read by using HP-IB secondary addresses 1, 2, and 3, or by sending special character sequences to the 2240A. HP-IB secondary addressing provides efficient transfer of any of the three status buffers with a single read statement. The special character sequences are provided for computers that do not support the HP-IB secondary addressing mode.

Firmware Architecture

The 2240A firmware is organized as three independent but cooperating tasks: an executive, an inbound message processor (IMP), and an outbound message processor (OMP). This multi-tasking architecture provides real-time advantages. For example, the message processors can handle requests for status information immediately, even though the executive is busy performing a measurement or control sequence. Fig. 3 presents the three tasks in state diagram form.

The primary responsibility of the executive is to execute requests and prepare results. It also performs automatic calibration of ADC (analog-to-digital converter) channels when signaled by a temperature change.

Fig. 4 delves more deeply into the executive state in which a request is executed. After initializing the condition code in the result buffer to zero, indicating no errors, the executive begins interpreting and executing commands in sequence. If the syntax of the current command is found to be correct, a command handler routine is called to execute that command. The normal exit from the request processor occurs when the request terminator character, !, is encountered. The result now contains the condition code and result data. Any error, such as an unrecognized command or recognition of a malfunctioning card, stops the request, changes the condition code to 1, and discards any data in the result.

In this fashion, a request always produces a result that is made available to the computer. If an error has occurred, the result contains only the condition code. The executive does no HP-IB communication itself; instead, it executes requests placed in the 2240A's buffer by the inbound message processor. Similarly, the result is accumulated in the buffer during the execution of a request and is transmitted by the outbound message processor. This interaction is shown graphically in Fig. 5.

The inbound message processor is responsible for the transfer of messages, one character at a time, from

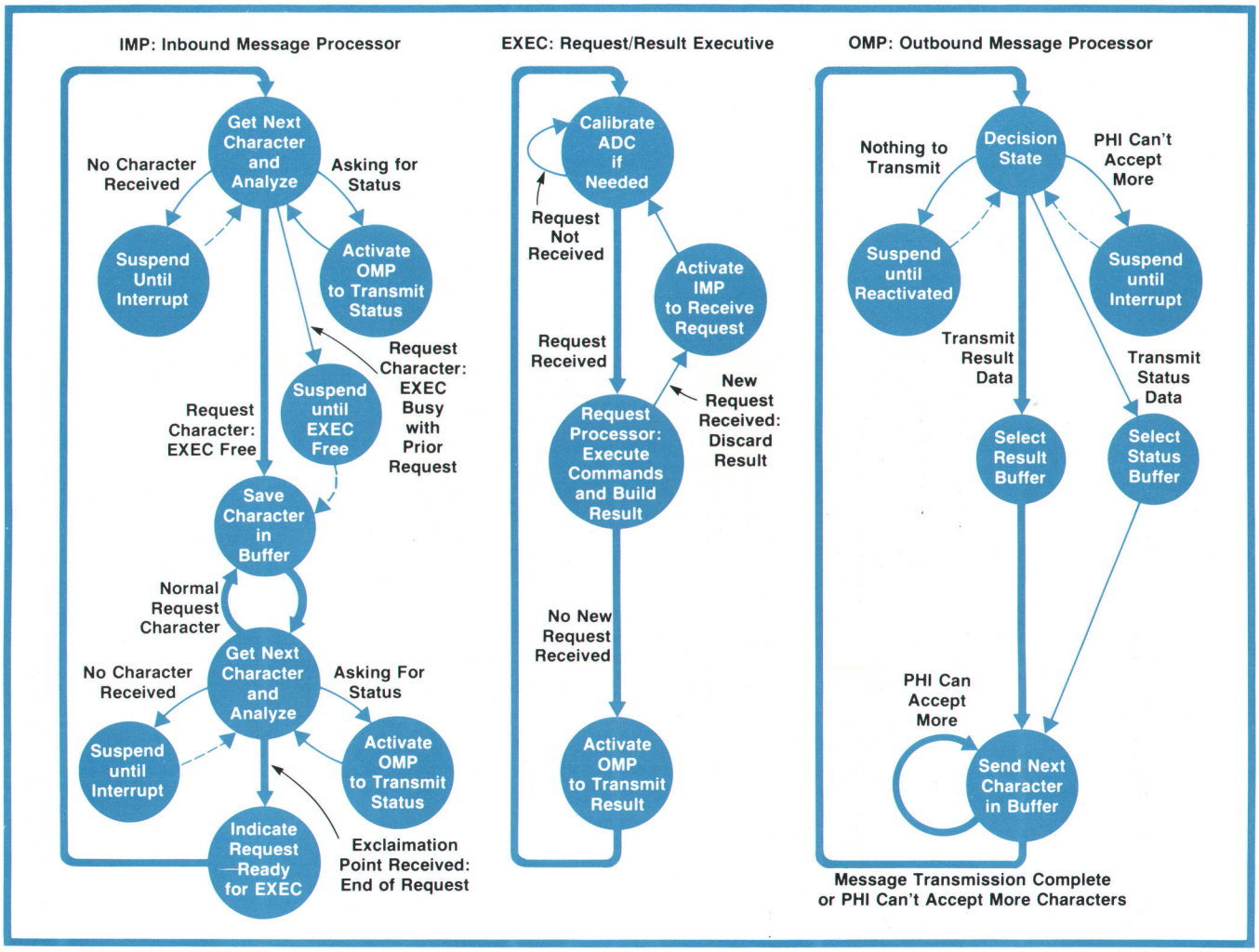


Fig. 3. *The 2240A is controlled by firmware programs stored in ROM. The firmware is organized as the three cooperating tasks shown here. The IMP is the highest-priority task and the EXEC is the lowest. A higher-priority task can preempt one of lower priority. Normal request/result flow is shown by the heavy lines.*

the HP-IB into the 2240A. Normally these characters are part of a request and are stored in the request buffer for the executive. To conserve buffer space, redundant blanks in the character stream are removed. When the request terminator character, !, is received, the inbound message processor signals to the executive that a complete request is available. The IMP must also watch for special characters or secondary addresses indicating status information is needed, and signal the outbound message processor to transmit the appropriate data.

The inbound message processor is normally interrupt driven and is activated whenever the PHI chip indicates that bytes are available on the HP-IB. When no more characters are immediately available, the IMP suspends itself until an interrupt indicates that at least one character has arrived. When characters are arriving but there is no place to put them, such as when a program sends a new request while an earlier one is still being executed, the inbound message processor suspends itself until the executive indicates the current request has been completely executed.

The outbound message processor transmits result or status messages to the computer over the HP-IB. It does this by placing eight characters at a time into a first-in first-out (FIFO) buffer on the PHI HP-IB interface chip. The OMP is also interrupt driven in that it suspends itself when the PHI cannot accept more bytes. When the PHI has transmitted the eight bytes, it interrupts the microprocessor to indicate that it has room for eight more. When the computer is accepting characters quickly, as with direct memory access, suspensions do not occur and the MC^2/PHI combination sustains a data rate greater than 200,000 characters per second.

Occasionally the transfer of a result by the outbound message processor is preempted by a status transfer. For example, the main program in the com-

Analog Input Card Calibration

by Vincent J. Dauciunas

Analog inputs to the 2240A are handled by the 22900A multiplexed analog-to-digital converter card. The 22900A provides for up to 32 single-ended or 16 differential high-level analog inputs, with a conversion rate of up to 20 kHz.

One of the important features of the 22900A is the ability to convert either a grounded input or a precision reference voltage. Another is the ability to sense temperature changes near critical components. Together these features allow the microprocessor to compensate analog readings for temperature drift.

The basic technique can be seen by referring to Fig. 1.* A differential-to-single-ended converter, a sample-and-hold amplifier, and a 12-bit successive approximation analog-to-digital converter form the heart of the conversion circuitry.

Each of the blocks is subject to errors as a result of offset voltage and gain changes as a function of time and temperature. Since the blocks are cascaded, the errors of a preceding block are modified by each succeeding block. To achieve high accuracy over the full operating temperature range, it is necessary either to use costly, stable, precision components, or to perform periodic calibrations. The 2240A takes the latter approach.

To calibrate the 22900A card, the following sequence is performed. Switch S1 is opened, and switches S3 and S4 are closed. This applies ground to the inputs of A1, and the resultant output, which is the total offset, is

$$E_o=((E_{o1}G_1+E_{o2})G_2+E_{o3})G_3.$$

This value is stored by the microprocessor. Next, S3 is opened and switch S2 is closed. This applies V_{Ref} to the inputs of A1, and the resultant output is:

$$V_o = (((V_{Ref} + E_{o1})G_1 + E_{o2})G_2 + E_{o3})G_3$$

$$V_o = G_1G_2G_3V_{Ref} + G_1G_2G_3E_{o1} + G_2G_3E_{o2} + G_3E_{o3}$$

A gain correction factor is computed by

$$G = \frac{V_{Ref}}{V_o - E_o}$$

$$= \frac{V_{Ref}}{G_1G_2G_3V_{Ref} + G_1G_2G_3E_{o1} + G_2G_3E_{o2} + G_3E_{o3} - G_1G_2G_3E_{o1} - G_2G_3E_{o2} - G_3E_{o3}}$$

$$= \frac{1}{G_1G_2G_3}$$

The microprocessor then stores this value. Next, switches S2 and S4 are opened and S1 is closed, connecting the inputs back to A1.

All succeeding readings from the 22900A are now processed by the microprocessor through the formula:

$$V_{correct} = G(V_{reading} - E_o)$$

which produces an output that is corrected for gain and offset errors. The microprocessor also checks that the values of G and E_o are within acceptable bounds. If they are not, an error message is generated, indicating a possible ADC card fault.

The 2240A allows for two modes of autocalibration: user-controlled or automatic. User-controlled autocalibration is initiated by the AC command, and is executed immediately. Automatic calibration is performed only when the on-card temperature, as determined by a temperature sensor, changes by a predetermined amount. The ADC card then generates an interrupt, and the microprocessor performs an autocalibration cycle. All succeeding readings from the card are corrected by the newly established correction factors until a user-requested or interrupt-generated calibration cycle results in a new set of correction factors.

The ability to switch in the ground or reference voltage through the use of several other low-level 2240A commands also yields a useful diagnostic tool in tracking down possible faults should there be a suspected problem with a 22900A card.

*A similar calibration principle is used in the 3455A Digital Voltmeter (Hewlett-Packard Journal, February 1977).

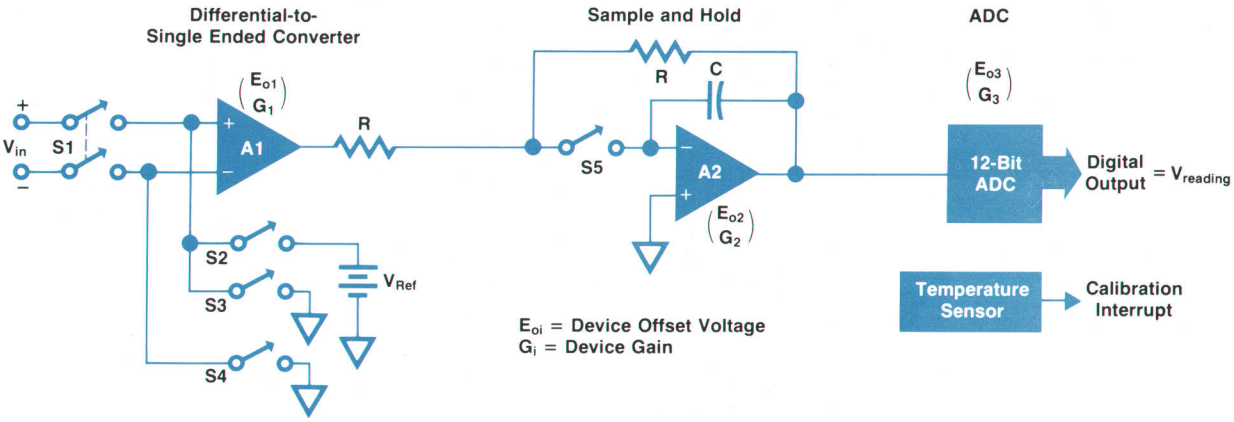


Fig. 1. *Simplified block diagram of the HP 22900A multiplexed analog-to-digital converter card. The card can convert a grounded input or a precision reference voltage and can sense temperature changes near critical components. These features allow the microprocessor to compensate readings for temperature drift.*

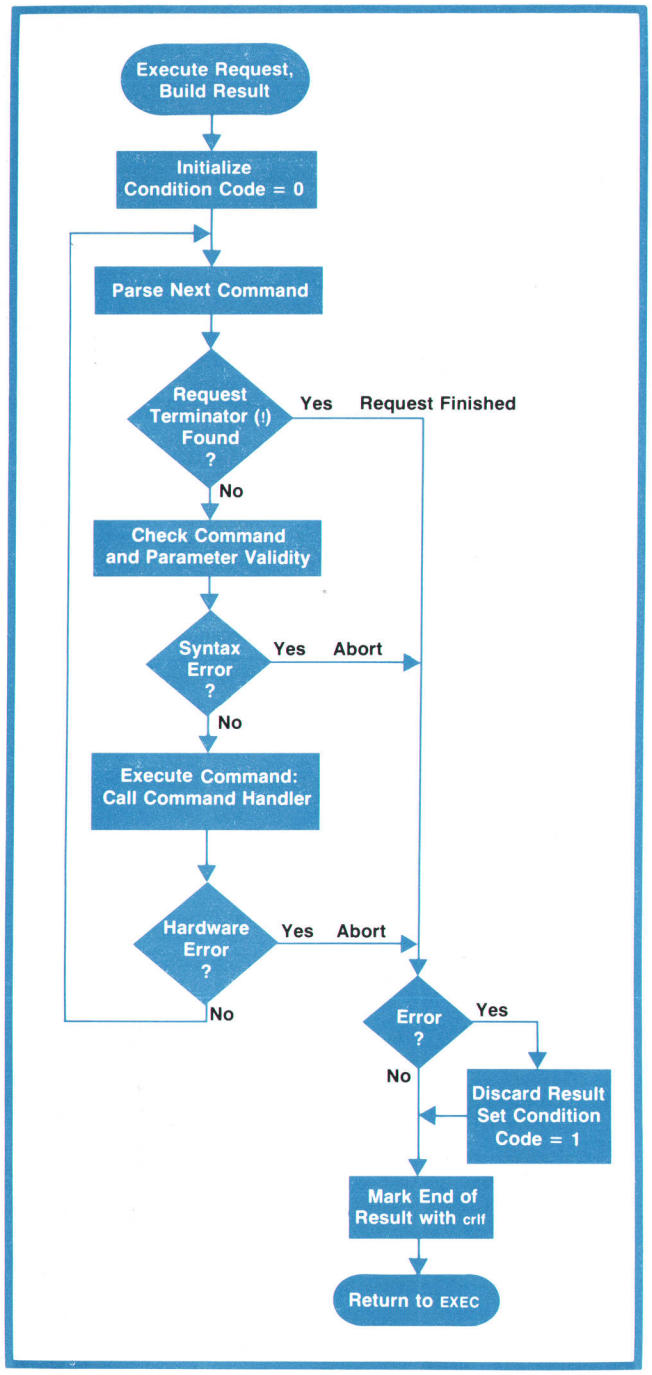


Fig. 4. *Request processing flow chart. Requests are processed by executing a series of commands in sequence. Command handler routines are called during request processing to execute various types of commands.*

puter might be reading the result from a scan of several sensors when the 2240A interrupts because a limit switch has tripped. An interrupt routine in the computer must then decide what caused the interrupt and whether it requires immediate corrective action. The necessary information is in the 2240A interrupt status buffer and is requested by sending the 2240A a status command in the form of an HP-IB secondary address. The arrival of this address immediately interlocks the PHI chip's outbound FIFO buffer so that none of the result characters will be accidently read by the interrupt routine. This gives the microprocessor time to gather the status information and place it in the outbound FIFO buffer, after saving any result data still in the FIFO buffer. After all the status information is accepted by the computer, the outbound processor resumes result transmission, and the main program continues, unaware of the entire transaction. If request execution is of higher priority than status response, the 2240A can be instructed not to respond to status reads until after execution of the request has been completed.

Verification and Self Test

A major concern of equipment users is how to verify that the equipment is functioning properly. In the 2240A this concern is addressed by two types of built-in service tools: self-test and function card verification.

The self-test runs whenever the 2240A is powered up, or upon command from the computer. It checks for proper operation of the microprocessor, ROM, RAM, PHI chip, interrupts, and function card interface circuits. In the ROM test, for example, MC^2 uses the contents of each ROM cell to compute a cyclic redundancy check code, which is then compared to the proper code stored on each page of memory. This test verifies that the contents of each ROM is correct and that the chips are loaded in the proper socket. The entire self-test sequence executes in less than three seconds.

The function card verification test is run to verify proper operation of the measurement and control cards and to diagnose any problems. To run these tests, the 2240A is switched off-line and a test fixture is connected to the rear of the instrument. This fixture simulates input signals and displays output signals. The test sequence is initiated by pressing a button on the front of the control card. The verification tests for the analog cards also provide a procedure for calibrating the cards. The technician can interact with the 2240A through switches and light-emitting-diode indicators on the test fixture and the control card. The flow chart of the analog-to-digital converter test is shown in Fig. 6.

Assuring Compatibility

The design objectives for the 2240A included direct plug-in compatibility with any HP-IB controller and language. A number of design features make this possible.

Messages, not Characters. 2240A communication is implemented and documented in terms of a few high-level "metamessages". Interaction at this level assures that subtle differences in command and data

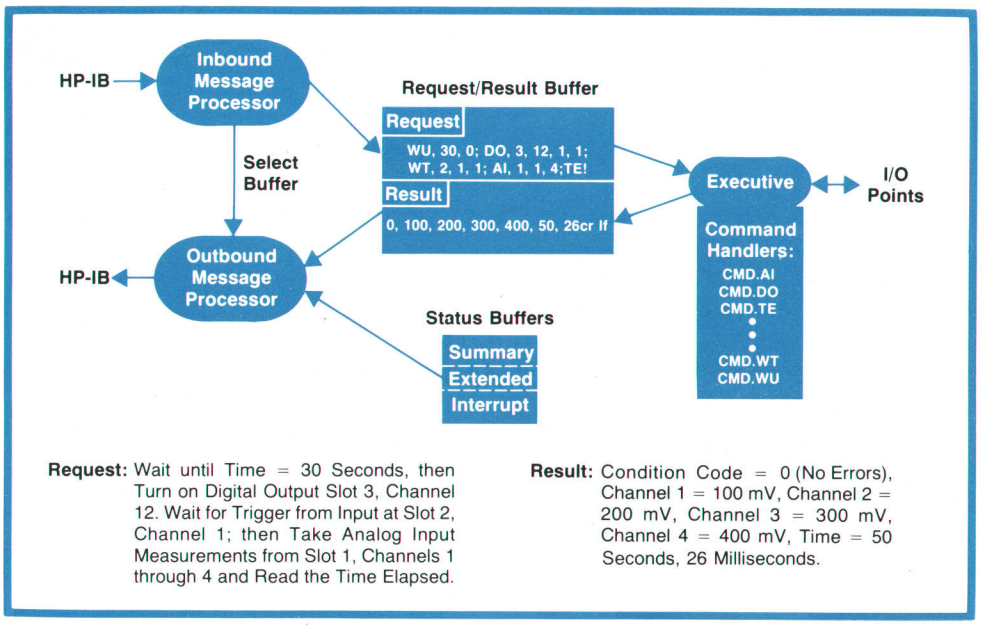


Fig. 5. *Message flow among the three 2240A firmware tasks.*

sequences will not preclude using the 2240A with a given controller. HP has begun describing the use and the capabilities of its computers and instruments in terms of messages transferred. This provides a common ground for relating any instrument to any computer. The objective is to allow the use of N instruments with M computers without writing N times M user's manuals. The 2240A uses the following HP-IB messages: data, clear, require service, status bit, and abort.

Computable Parameters. Careful consideration to parameter format assures straightforward programming. Consider the request: AB,3,4,1,−100!. This analog bipolar output command will cause −100 millivolts to be produced at the connection to channel 4 of the digital-to-analog converter in slot 3. This seems simple enough, but more often than not some or all parameters are computed and come from program variables instead of ASCII constants. This usually results in a character sequence such as:

```
AB, 3    3.99999    1,    −100.37    !
```

This has exactly the same effect as the previous request. The 2240A rounds the 3.99999 to 4, the −100.37 to −100, and is tolerant of the extra delimiters. Difficult-to-compute formats, such as 100− for negative voltages and 3.4 for slot 3 channel 4, have been avoided.

Flexible Request Syntax. Some peripherals require that the programmer precisely control the data format of a WRITE or other output statement. The 2240A relieves the programmer of these concerns by accepting anything that a person can read unambiguously. Commands and data may be surrounded by leading and trailing blanks. Spaces, commas, and semicolons may be freely used as delimiters, and upper or lower case letters are acceptable for commands. While delimiters make a request more readable, they are required only between adjacent numeric fields.

Explicit Request Terminators. The exclamation point (!) was chosen as the request terminator to avoid a programming complication. While most computers send the ASCII carriage return and line feed (cr lf) characters at the end of a message, suggesting their use as a message terminator, some do not. Still others send cr lf in the middle of messages, after every few numeric fields. The 2240A ignores cr lf sequences and continues to accept request characters until ! is received. This convention frees the programmer from concern with the cr lf conventions of the computer. It is particularly convenient to know that cr lf is ignored when multiple write statements are used to send arrays of data within a request.

Universal Result Format. The result carries measurement, timing and error information to the computer. All 2240A quantities are expressed as integers and transmitted in standard free-field ASCII format. This format is acceptable to all current HP computers that support the HP-IB. The 2240A will pad the result with zeros and commas to the extent required to satisfy a read statement that asks for too much data. This normally occurs after an error terminates a request but the program expects measurements in the result. Padding avoids a potential "hang-up" situation.

Respect for Buffer Size. While the 2240A can produce a result nearly 1600 characters long, some languages restrict the number of characters that may be transferred by a single read statement. This limitation

PHI, the HP-IB Interface Chip

by John W. Figueroa

In the 2240A Measurement and Control Processor, the interface between the MC² microprocessor and the HP-IB is implemented by a single LSI CMOS/SOS chip* called PHI (processor to HP-IB interface). Although well suited for its HP 2240A application, it has more general capabilities, including the entire logic interface of IEEE standard 488-1975.

How the HP-IB standard became the PHI chip makes an interesting story. Since it had been an early goal of HP's Data Systems Division to standardize peripheral interfaces, the division in 1972 contributed modifications to the proposed HP-IB standard that made it better suited to computer systems. Unfortunately, this introduced further complexity and made it likely that multiple independent implementations of the HP-IB would result in system level problems.

The talker/listener functions of the HP-IB, needed by peripherals and instruments alike, could be readily implemented with discrete IC logic. However, the full controller function and processor interface needed by the computer I/O channel added considerable logic to the design. At that time, only small and medium-scale integrated circuits were available to implement the added logic. The resulting increase in size of the interface, a higher manufacturing cost, and longer and more costly development were not acceptable in the long run.

The solution to these problems was obviously an LSI chip, but the technology for a large, random logic design fast enough for tape drives and discs was not to be available until years later with the emergence of HP's CMOS/SOS technology. With the proper technology it became possible to produce the PHI chip. PHI is destined to be used in the design of a new generation of microprocessor-driven controllers, peripherals, and instruments.

PHI Architecture

The PHI chip provides a microprocessor I/O interface organized around seven registers for interrupt, control, and status, as well as two independent first-in first out (FIFO) data buffers. Fig. 1 is the block diagram of the PHI chip.

The processor bus operates with either 5-volt TTL or 12-volt MOS microprocessors. It is ideally suited for use with the HP 16-bit CMOS/SOS microprocessor but also operates with minimal additional logic with most 8-to-16-bit microprocessors. The HP-IB side is standard and will not be described here.

Maskable processor interrupts and DMA handshake are implemented, allowing PHI to operate in parallel with and independently of the microprocessor. These features enhance the total microsystem's performance, effectively freeing the processor from the details of the HP-IB I/O.

There are nine distinct bits in the first-level priority interrupt register. A tenth bit is the logical OR of the other nine and connects to the processor interrupt line. All ten bits are individually maskable. If appropriate, they are individually clearable by the processor.

The outbound FIFO buffer in a controller PHI allows queueing of HP-IB commands and macrocommands that direct the transfer of data sent by other talkers over the HP-IB at the full one-megabyte rate. The macros allow synchronous control by virtue of the controller PHI's participating in every handshake. The three macrocommands provided are an uncounted transfer terminated by the HP-IB EOI bit, a counted transfer terminated by count=0 or by EOI, and a counted transfer terminated as above or by a line feed. Counted transfers larger than 256 bytes are handled by automatic chaining of macrocommands from the outbound FIFO buffer.

When the outbound FIFO buffer in a controller PHI is empty, the PHI saves time by automatically conducting a continuous parallel poll operation. This poll is terminated as soon as the processor writes a word into the outbound FIFO buffer.

The parallel poll responses are maskable and normalized for high/low polarity for each bit. The resulting eight bits are available to the processor as a second priority level of interrupts. The logical OR of all the masked responses constitutes a first-level priority interrupt.

A programmable two-byte identify capability is provided to allow a computer acting as an HP-IB controller to find out via the HP-IB what peripherals or instruments are currently connected to its HP-IB I/O system.

The remaining programmable PHI registers handle the HP-IB address and miscellaneous control and status bits for normal and diagnostic operation.

(Continued on next page.)

*An LSI CMOS/SOS chip is a large-scale integrated circuit chip made by the complementary metal-oxide-semiconductor silicon-on-sapphire process.

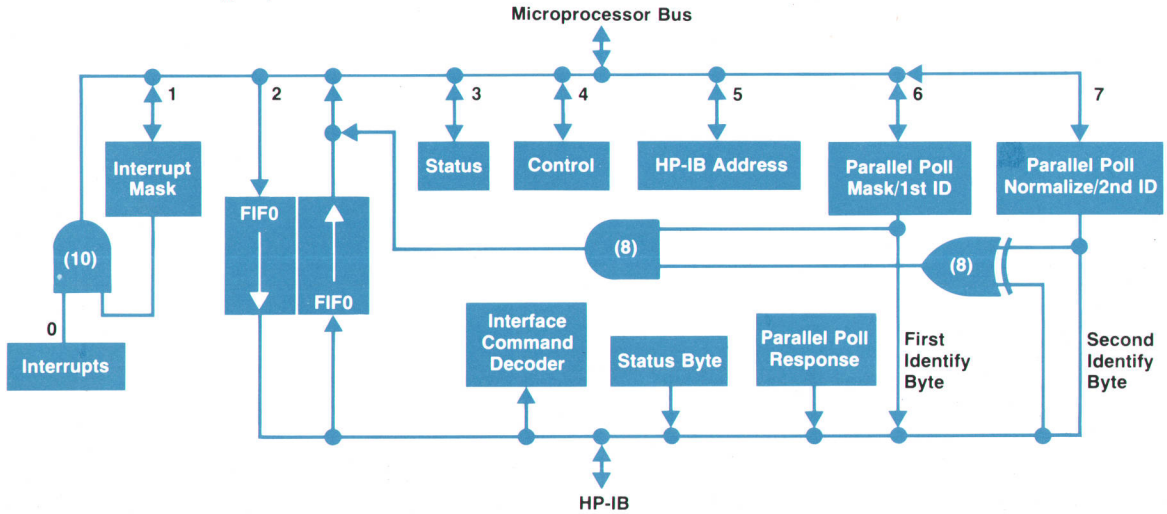


Fig. 1. *Block diagram of the PHI chip. The chip implements the entire logic interface of IEEE 488-1975.*

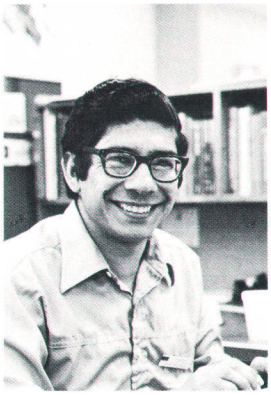
Diagnostic Capabilities

A programmable off-line state as well as FIFO buffer wraparound (from outbound to inbound) are part of the extensive diagnostic capabilities provided. Most registers can be written to and read from to assist in firmware debugging. The off-line test can be done totally by software without disconnecting the PHI from a working HP-IB system. The 2240A uses this feature in its self test.

Unlike the HP-IB handshake, the processor handshake will not freeze the processor bus if the data transfer cannot be executed. In lieu of waiting, a FIFO operation completes without a real data transfer and is followed by an interrupt. This allows efficient firmware debugging and error recovery.

Separate parity generator and checker logic is provided for HP-IB commands. A parity error generates a maskable interrupt but allows execution of the HP-IB command.

For further parity error control, a programmable control bit allows freezing of the HP-IB handshake and reading of the HP-IB DIO lines, but does not execute the questionable command. Normal operation goes on when the transient disappears, when the controller times out (not a PHI function), or when the receiving PHI is reset.



John W. Figueroa

John Figueroa joined HP in 1969 with a BSEE degree from the University of Florida. After writing much automatic test software and managing a programming group, John transferred in 1972 to HP's Data Systems Division to work on the new computers being developed. An early advocate of the HP-IB for computer I/O, he became a group manager for HP 3000 hardware and then for HP 2000 Systems. Since 1975, John has been doing R&D on the MC² and PHI LSI chips while pursuing his MSEE at Stanford University (he received it last month). He is married, has two sons, and enjoys chess, skiing, science fiction, and driving his 1961 Corvette.

normally arises because of a small buffer in the computer's memory, often only 80 to 144 characters long. Reading a long message into a short buffer usually results in loss of most of the message. The 2240A compensates for this by breaking a long result into several smaller messages when necessary. Two commands are provided to control this blocking feature.

Transparent Multiplexing of the HP-IB. The normal data flow between a computer program and an instrument may be broken by an interrupt that signals an unusual event and invokes a special interrupt service program. Such a program can immediately interrogate the status buffers of the 2240A for various information, such as the cause of the interrupt and the command currently being executed. The interrupt program can use HP-IB secondary addressing to read from the status buffers. When the main program continues, it will not see any effect of the interruption, even if it occurred in the middle of a request or result transmission.

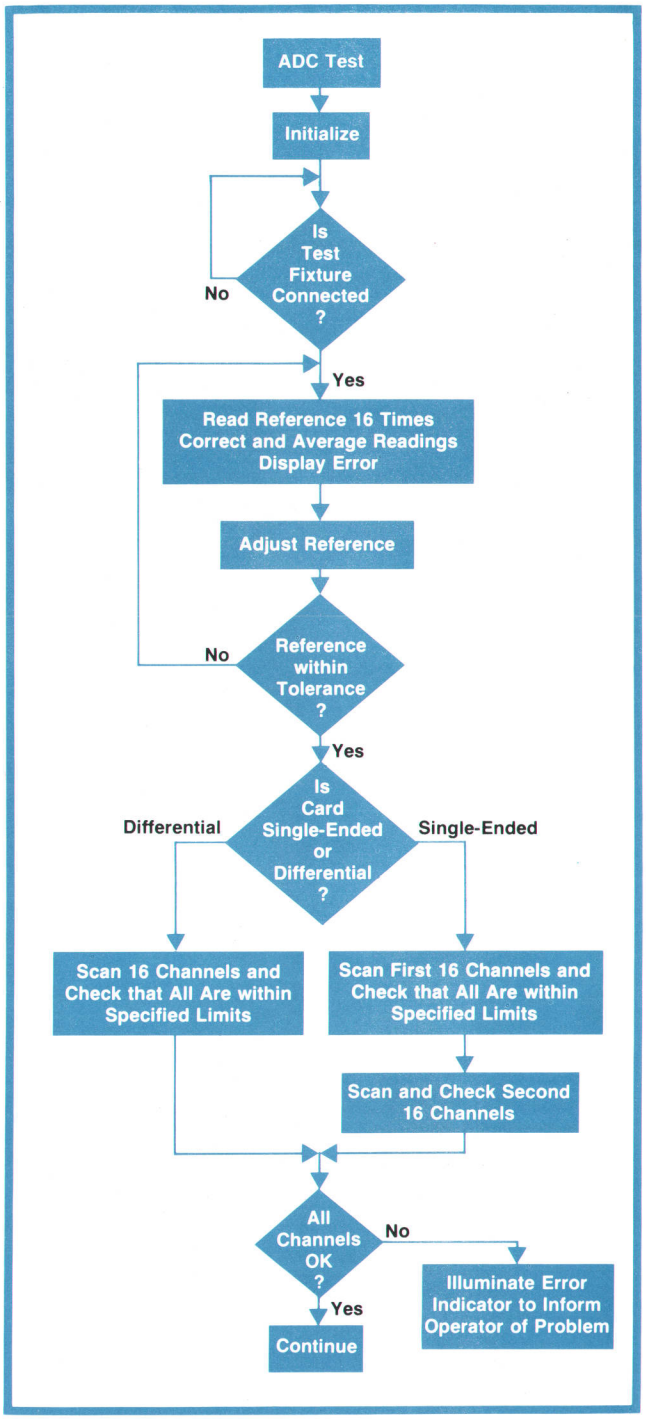


Fig. 6. *Self-test and function card verification tests are built into the 2240A firmware. This is the flow chart of the verification test of the analog-to-digital converter input card.*

Alternative for Secondary Addressing. The 2240A is accessed via its primary HP-IB address for transmitting requests and reading results. A secondary address is sent along with the primary address for reading status information. The secondary address affords an unambiguous selection of a status buffer and transfer of its contents with a single read statement. Since

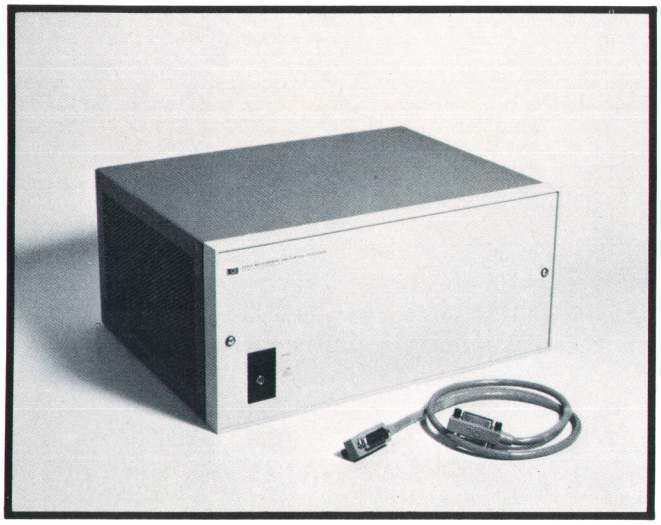


Fig. 7. *HP Model 2240A Measurement and Control Processor.*

some computers or languages may not support secondary addressing, a scheme was devised for them to simulate secondary addresses. The following sequence, written in HP BASIC, simulates a read from secondary address 2, the 2240A's extended status buffer:

PRINT #12; "$T2"	Send special command for status reading
READ #12; A, B, C, D	Read status information

The $T... sequence is treated as a special case by the 2240A. It means secondary ($) talker (T) number two (2). While not currently used, $L... could simulate a secondary listener selecting the target of a data transfer.

Block-Oriented Transfers. Computers operate most efficiently when I/O operations deal with blocks of data, usually via direct memory access channels, instead of programmatically with individual bytes. Intelligent peripherals can store and process large amounts of data and are therefore compatible with block transfers. The 2240A request/result protocol is designed to encourage block transfers. The 2240A can receive a request at 70,000 bytes per second and transmit a result at 200,000 bytes per second.

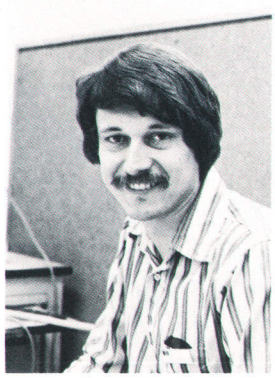
Acknowledgments

The author wishes to acknowledge the many efforts of the other members of the controller team. Ray Brubaker made major contributions to the control card hardware as well as firmware architecture and design. As primary backplane architect, John Wiese designed the function card interface hardware on the control card, as well as verification and self-test firmware. Vic Hardy designed the verification test fixture and verification firmware. Terry Leuthner implemented the ADC calibration firmware and spent many hours on software testing.

Special thanks go to Fred Johnstone as author of the excellent 2240A user's manual.

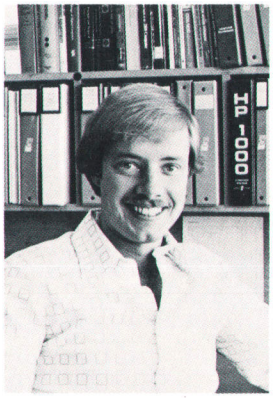
References

1. R.H. Brubaker, Jr. and D.E. Klaiss, "Microprocessor Intelligence in Instrumentation Simplifies Computer Software," Proceedings of the Instrument Society of America Conference, Niagara Falls, N.Y., October 17-20, 1977.
2. B. Forbes, 'Silicon-on-Sapphire Technology Produces High-Speed Single-Chip Processor," Hewlett-Packard Journal, April 1977.



Vincent J. Dauciunas

Vince Dauciunas received his BSEE degree from the University of Notre Dame in 1972 and his MSEE from the University of California at Berkeley in 1974. During his student years, he worked on ground receivers for deep-space tracking and served as a teaching assistant. With HP since 1974, he's the designer of the 22900A ADC card for the 2240A Measurement and Control Processor. Vince was born in Culver City, California. He's married, lives in Santa Clara, California, and enjoys radio-controlled sailplanes, volleyball, and photography. He's a member of IEEE.



Donald E. Klaiss

Don Klaiss joined HP's Microwave Systems Lab in 1973 after receiving a BSEE degree from Rutgers University in New Jersey. He received his MSEE degree from Stanford University in 1975 and is currently pursuing an MBA at Santa Clara University. He has been involved in the design of several HP products including the 8542B Automatic Network Analyzer and the ARS-400 automatic spectrum analysis and receiver system. He had major responsibility for HP-MCL firmware design for the 2240A Measurement and Control Processor. Don is now responsible for measurement and control firmware development at HP's Data Systems Division. He has published technical articles and is a member of the IEEE Computer Society. Don is single, lives in Mountain View, and enjoys tennis, volleyball, camping, music, theater, and playing piano and guitar.

An Easy-to-Use Data Capture Terminal for Industrial Operations

Designed for collecting data at remote points within a manufacturing operation, this compact terminal is operated easily by those unfamiliar with computer operations. It can also serve as a link between a computer and distant HP-IB-controlled instruments.

by Jacques A. Ripert, Daniel C. Berthier, and Michel E. Bernard

DATA COLLECTION OPERATIONS are found in an extremely wide variety of situations—manufacturing, inventory control, point of sale, hospitals, to name a few.

The characteristics of these different applications are such that no one terminal satisfies the needs of all. Therefore, when the design of new terminals for data collection was undertaken at HP, strict attention was paid to fulfilling the needs of the industrial environment, the intended area of application for these terminals.

The principal characteristics of the industrial environment are as follows.

- A great variety of tasks are performed simultaneously in different parts of the factory. In general, decisions or actions related to these tasks are based on the latest information received, so it is highly desirable to collect data on a real-time basis.
- Users of the terminals are not data-processing specialists. They must perceive the terminals as a help and not as a nuisance that complicates their work.
- Necessary information is generated wherever the work is done, so the cost of cabling and the ease of installation could become significant factors in the total investment in a data-collection system.
- Factory needs change, so a terminal should be capable of being relocated easily without major changes in the cabling. Hence, ease of connection also assumes primary importance.
- The fact that one terminal is turned on or off or connected or disconnected while the system is operating should not affect the operation of the others. Each terminal should be independent of the others.
- Motor starting controls, arc welders, and other sources of electrical transients create an electrically hostile environment. Since an error in transmitted data could have dramatic consequences, the data transmission system must have high noise immunity.
- It is often desirable to collect data such as temperatures, pressures, and voltages automatically from test stations distributed throughout the plant. In addition, it may be desirable to control the test instruments from a central location.

These considerations influenced the design of the HP Model 3070B Terminal (Fig. 1) and the data collection system with which it works.

Characteristics of the System

The data collection system that this terminal is to be used with is based on the HP 1000 System,[1] a family of small computer systems using real-time executive (RTE) operating control software. These systems are well suited to computational, process control, automated/test measurement, and operations management applications. They can also serve as the central computer in distributed systems networks.[2]

As many as 56 Model 3070B Terminals may connect anywhere desired to a single, shielded, twisted-pair cable. To avoid the need for additional conductors, no clock signal is transmitted. Instead, a method of using the transmitted data for synchronization was devised.

The system's computer may also connect anywhere on the cable. The total cable length can be up to four kilometers provided that no terminal is more than two kilometers from the computer. There is no need for repeaters on the cable and there is no need for relays to maintain a through connection for any terminal that may be turned off.

The connection boxes where the terminals connect to the cable were designed to allow any terminal to be connected or disconnected without disturbing the transmission of data from the others. Connection to each terminal is made through optical isolators to avoid the formation of ground loops. In addition, any terminal may be turned on or off without affecting the functioning of the others or the integrity of data they may be transmitting.

Fig. 1. *The new Model 3070B Terminal is a compact, desktop device that can fit unobtrusively into a working environment. With user-defined labels on the 10 keys and 15 prompting lights, no special training is needed to learn to use the terminal.*

To minimize the effects of electrical disturbances, the twin cable conductors are driven differentially. Also, information is transmitted in an error-detecting code and the protocol for information exchange further enhances reliability. The protocol is handled at the computer by a special I/O card designed for use with HP 2100-Series Computers.

HP-IB Compatibility

The new terminal is compatible with the HP Interface Bus,* allowing up to 13 instruments to be connected to each terminal for measurements of temperature, pressure, voltage, etc. Each terminal may thus relay commands from the computer to the instruments and return to the computer the resulting data, such as minute-by-minute power consumption, conveyor-belt speed, and so on. In effect, the new terminal extends the permissible distance between the computer and the HP-IB instruments to 2 km (1.2 miles) from the 20 meters allowed by direct connection. In particular, Model 3070B provides a convenient means of linking one or more Model 2240A Measurement and Control Processors to a computer (see the article on page 2). The terminal's HP-IB interface also enables it to work with HP-IB compatible desktop computers, which could serve as data preprocessors for the computer.

Characteristics of the Terminals

The Model 3070B Terminal has a numeric keypad, ten special function keys, fifteen prompting lights, and a 15-character LED display. Each prompting light, which is turned on by a single ASCII character sent by the computer, represents information or a command to guide the user through a transaction. By choosing the appropriate special function key, the user can respond to the command or initiate a particular action. Nomenclature for the keys and lights, assigned by the computer program, can be written on a paper label that is inserted underneath a protective transparent plastic overlay. The nomenclature is thus easily adapted to the particular application of the terminals.

Model 3070B has a 20-character-per-line thermal printer that can provide a hard copy of transactions on the terminal, such as work done and parts shipped, or it can be used to print routing slips, shelf storage numbers, etc. It has a set of 64 characters.

The new terminal also has a multifunction reader that can read three types of documents:

(1) Type-3 Hollerith punched badges. These can be used to identify the user for gaining access to the system, or they can be used to identify a particular operation, machine, or test station.

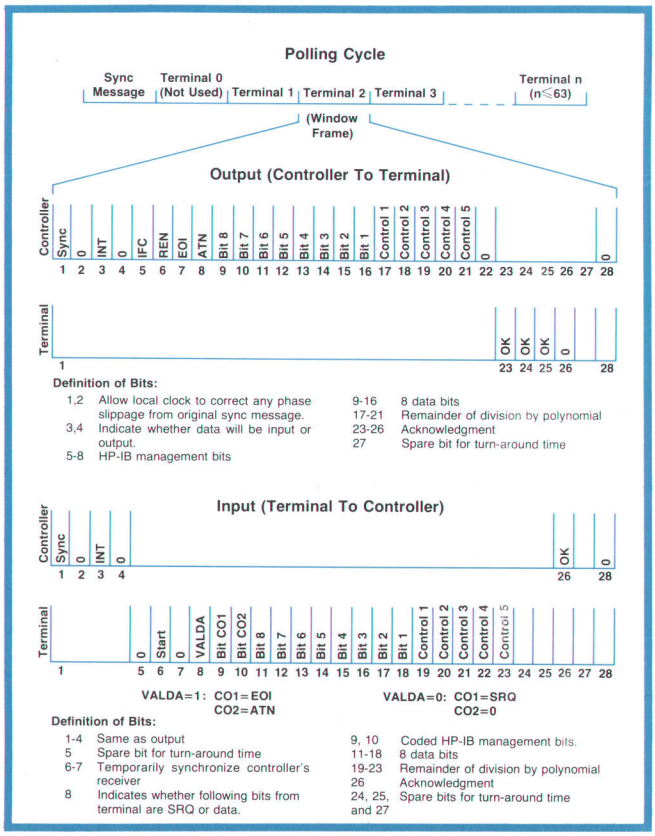


Fig. 2. *Timing diagrams for communications protocol show message formats for incoming and outgoing data. The polling cycles have one time window for each terminal connected to the serial link cable. Up to 63 terminals can be connected to one cable (56 with HP 1000-series systems).*

*Hewlett-Packard's implementation of IEEE Standard 488-1975 and ANSI Standard MC1.1.

(2) Standard 80-column punched cards. These can travel with work in progress to ensure that identification numbers are entered into each terminal correctly.

(3) Marked cards. These can serve as source documents for areas that do not have immediate access to the terminals. They can be punched as well as marked, the perforations representing fixed data that is augmented by pencil marks made by the user.

The reader can be programmed to respond to only punched holes. Thus it can read punched cards that are soiled or that have writing on them (see box).

The Serial Link

The protocol for data transfer between the system computer and distant 3070B terminals is designed to achieve maximum transmission reliability. It is based on repetitive polling cycles initiated by the computer. As shown in the diagram of Fig. 2, each polling cycle

A Multifunction Reader

The reader in the Model 3070B Terminal can read both marks and punched holes on the same card. Alternatively, it can be programmed to read only holes, which enables it to read punched cards that are dirty or that have writing on them.

A diagram of one of the optical reading elements is shown in Fig 1. There are thirteen of these in the card reader, twelve for the twelve rows of holes on standard Hollerith cards, and one for a clock track that may be printed on some cards.

In a reading element, infrared radiation generated by a light-emitting diode (LED) is conducted to a card by a fiber-optic light guide. Light reflected from the card is carried by a second light guide to a phototransistor. The surface of the card reflects only part of the LED illumination, so the output of the phototransistor circuit will then be at a midrange voltage level, V_{norm}, as shown in Fig. 2a. When a punched hole passes over the light guides, the LED illumination passing through the hole is totally reflected by a mirror, causing the phototransistor circuit output to go to the saturation level, V_{max}. On the other hand, a mark on a card absorbs the LED illumination, so the phototransistor circuit output drops to a low level, V_{min}.

The detection circuitry is shown in Fig. 2c. The output, V, of the phototransistor circuit is applied to one input of a comparator. The voltage, V_i, at the comparator's other input is derived from V by way of an attenuator and a low-pass filter. As shown by the waveforms in Fig. 2b, in the steady state V is at a higher voltage level than V_i and the output of the comparator is high. However, whenever there is a negative-going transition in V that is faster than the time constant of the low-pass filter, the delay in V_i allows V to go below V_i, and the output of the comparator goes low. As shown by the diagrams of Fig. 2b, both holes and marks thus cause negative-going pulses at the output of the comparator.

The comparator sets a flip-flop that is clocked by pulses derived from a code wheel on the drive motor, thus matching the reading speed of Hollerith cards that have normal column-to-column spacing (80-column density). Alternatively, the flip-flop can be clocked by pulses derived from clock marks printed on the lower edge of a card.

The outputs of the flip-flops for all channels are applied to a converter (not shown) that generates ASCII characters in response to the standard Hollerith card code. Alternatively, all twelve channels can go directly to the microprocessor bus in two consecutive 6-bit bytes. These are then converted to two ASCII characters, the "image" of the 12-bit binary number represented by the holes in a column. The characters are transferred on the bus to a buffer memory that holds up to 160 characters.

Gates symbolically represented by Switch S1 in Fig. 2c can set a threshold that prevents the reader from responding to marks on a card. With the switch in the "holes only" mode, the lower excursion of V is clamped at a level higher than V_{norm}, so marks generate no output. Besides enabling the reader to read soiled cards, this arrangement allows comments to be written on a card with no danger of causing false outputs.

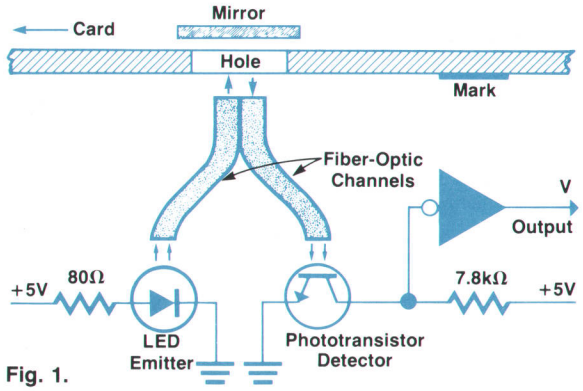


Fig. 1.

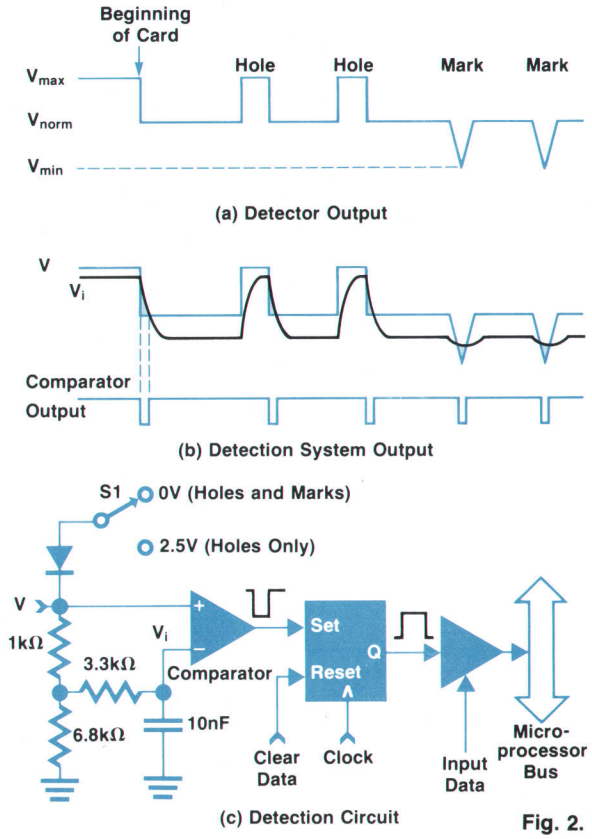


Fig. 2.

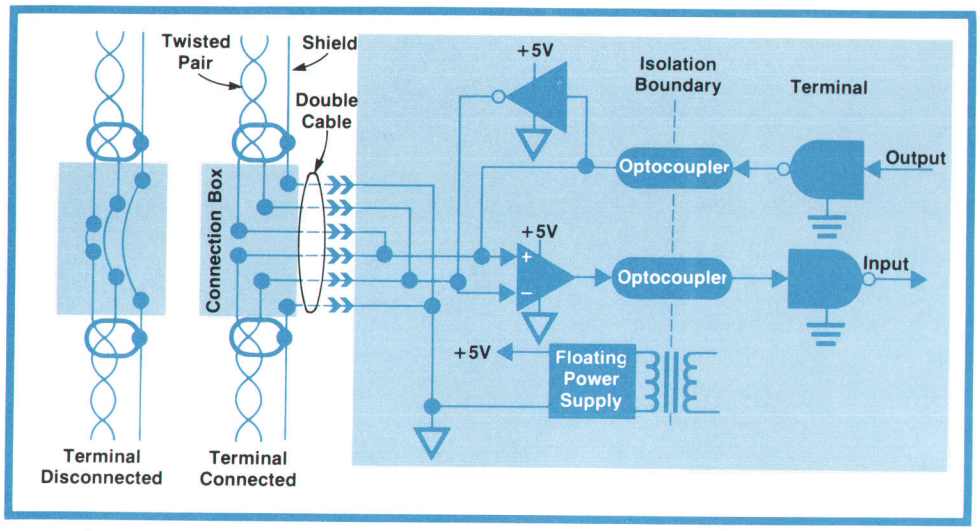


Fig. 3. *Simplified diagram of the connection between a terminal and the twisted-pair cable. Data is transferred in and out of the terminal through optocouplers to prevent the formation of ground loops.*

has a series of time windows each of which is assigned to a particular terminal. During a polling cycle, each terminal can transmit or receive one 8-bit ASCII character during its allotted time window.

The rate at which polling cycles occur depends on the number of terminals in the system and, hence, on the number of time windows in the polling cycles. For example, with 32 terminals, polling cycles occur 26 times per second, i.e., each terminal can send and receive at a rate of 26 characters per second. With just one terminal, the rate is 280 per second.

Operation between the terminals and the computer is coordinated by a sync message sent by the computer at the start of a polling cycle. This message consists of a "1" followed by 32 "0's". Since 32 consecutive 0's do not occur during normal traffic, the terminals can recognize this as the sync message. At the same time, a counter in each terminal is reset and starts counting time windows to determine when the timing window for that terminal occurs. Terminals adjust their clocks to be in phase with the sync bit of the sync message.

A 5-bit error-checking message is appended to each character (see Fig. 2) in the form of a cyclic redundancy check. This message is derived by dividing the 13-bit data message (8-bit ASCII character plus five HP-IB control bits) by the binary polynomial $x^5 + x^2 + x + 1$. The remainder resulting from the division is transmitted as the error-checking message. At the receiving end, the entire 18-bit data code (13 bits plus 5-bit error-checking message) is divided by the same polynomial and if the remainder is other than zero, an error is indicated.

The receipt of each character at its destination (terminal or computer) is acknowledged by the transmission of an OK code by the receiver. In the event of a transmission error, a not OK ($\overline{\text{OK}}$) is transmitted and the sender retransmits the character during the next polling cycle.

Transmission reliability is further enhanced by sampling each bit eight times at the receiver. During the eighth sample, a majority "vote" is taken on the first seven samples to decide whether the bit is a 1 or a 0. The SYNC and START bits, however, must register seven consecutive 1's to be declared a 1. This assures terminal synchronization to within one-eighth of a bit.

Data is transmitted as 5-volt, NRZ pulses at a bit rate of 25 kHz. Propagation delays and phase delays between the computer and terminal clocks could cause delays in bits received at the computer. When the computer interface is listening for an input, it temporarily goes into an asynchronous mode and waits for the START bit from the terminal to synchronize its receiving circuits. However, the main clock continues without change so the next time window remains synchronized to it and thus to the start of the polling cycle.

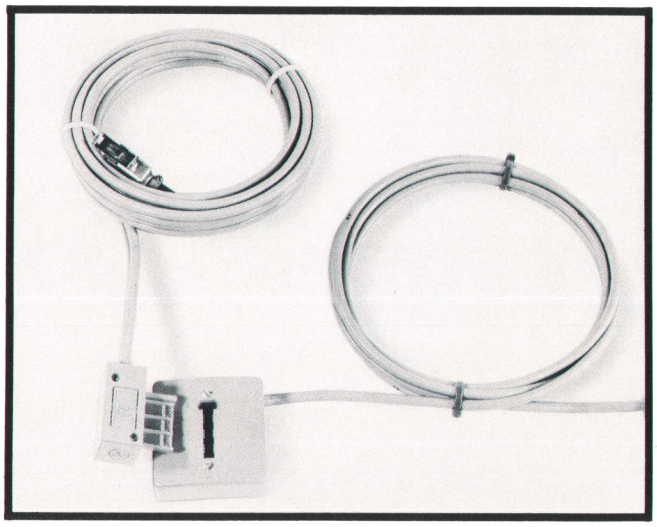


Fig. 4. *Connection boxes may be placed anywhere on the serial link cable. A terminal's connecting cable plugs in with a make-before-break-operation that does not interefere with transactions being conducted by other terminals on the cable.*

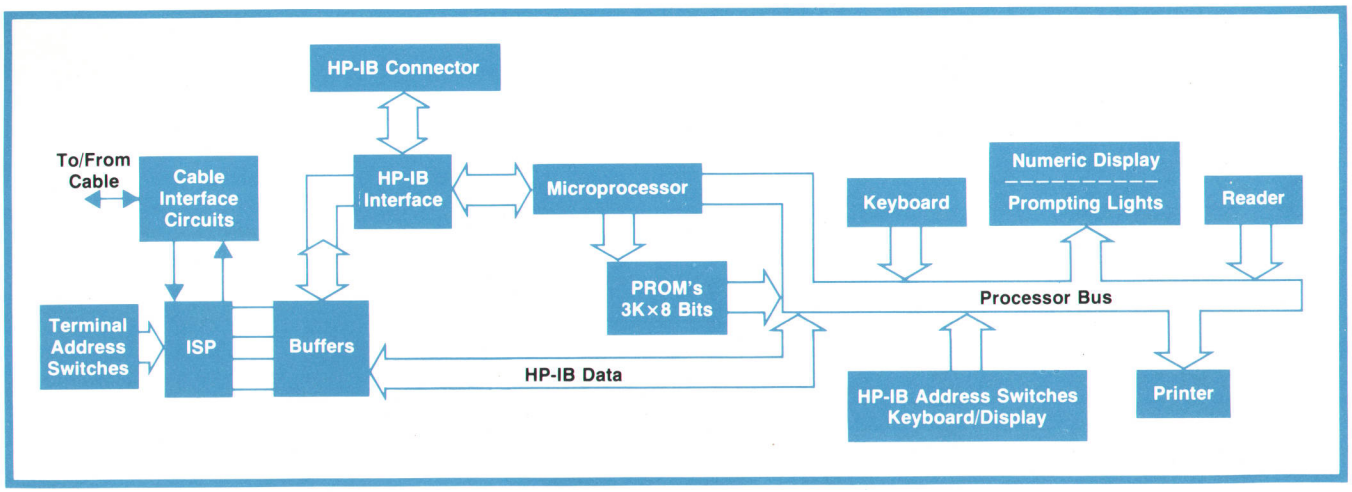


Fig. 5. *Block diagram of Model 3070B Terminal.*

The Hardware

A diagram of how a terminal connects to the cable is shown in Fig. 3. Connection boxes, shown in Fig. 4, may be placed anywhere desired along the cable. When a terminal is not plugged into a connection box, a through connection is maintained for the cable. When a terminal is plugged in, the through links are disconnected and a double cable is inserted, effectively rerouting the twisted pair to the connector on the terminal. This minimizes cable impedance discontinuities by keeping the terminal's input leads as short as possible. Plugging into the connection box is a make-before-break operation so cable continuity is never interrupted by connecting or disconnecting a terminal.

The input and output amplifiers in the terminal are isolated from the rest of the terminal circuits by optocouplers and a floating power supply. The input amplifier has a high impedance so as not to load the cable. The output amplifier is a low-impedance current driver that is turned off when not transmitting so it will present a high impedance to the cable.

The input and output signals are processed through the ISP (Interface Serial-Parallel) module (see block diagram of Fig. 5). This is a custom-designed large-scale integrated circuit that converts the incoming serial data to the HP-IB parallel code and the outgoing HP-IB code to serial. In addition, it generates the error-checking message for the output and checks incoming code for correctness. Also included in the ISP is the counter that determines which window frame in the polling cycle pertains to that terminal.

Incoming messages for the terminal processed by the ISP are applied to, and outgoing messages are obtained from, the terminal's microprocessor, an HP-designed 8-bit device. This microprocessor controls all the terminal's modules. It also performs a self-test procedure on request.

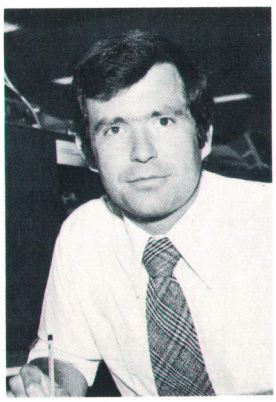
Each of the terminal's sections (keyboard, display, printer, card reader) can be configured separately as a talker or listener on any HP-IB system connected to the terminal. However, for transactions between the computer and the HP-IB system, the ISP simply serves as an interface and the terminal is essentially transparent to computer/HP-IB communications.

Acknowledgments

Special thanks are due Paul Febvre, now at HP's Fort Collins Division, who initially developed the 3070 concept. Special thanks are also due Jack Magri who designed the mechanism of the multifunction reader and did a superb job in fitting it and the printer into a small enclosure. And finally, we wish to thank all the members of the Grenoble Division who by their efforts, in the lab, in marketing, and in production, contributed to the realization of the 3070B.

References

1. L. Johnson, "A New Series of Small Computer Systems," Hewlett-Packard Journal, March 1977.
2. R.R. Shatzer, "Distributed Systems/1000," Hewlett-Packard Journal, March 1978.



Michel E. Bernard

Michel Bernard graduated from the Ecole Nationale Supérieur d'Arts et Métiers, worked for a year, then obtained an MSEE at Stanford University (1971). He spent a year in the French Army then joined HP France, subsequently becoming project leader for the 3070-series terminals. He is now with the customer service division in Grenoble. The son of a grape grower, Michel enjoys wine tasting, hiking, skiing, and traveling in remote parts of the world (Afghanistan, Nepal, etc.).

Jacques A. Ripert

Jacques Ripert joined HP France in 1974. He was architect of the 3070 serial-link protocol, defined the ISP IC, and did much of the basic terminal's electronic design. Jacques started his career in 1967 as a technician in the electronics lab of the French Atomic Energy Commission. He attended night classes in electronic engineering, designed a frequency-to-voltage converter IC for an industrial firm as part of his course of study, and passed national exams that earned him the degree of Ingénieur du Conservatoire National des Arts et Métiers. Besides taking care of his beehives, Jacques spends his free time skiing, canoeing, and bicycle riding with his wife.

Daniel C. Berthier

Daniel Berthier graduated from the Grenoble School of Engineering in 1964 and did postgraduate studies (roughly the equivalent of an MSEE) at the University of Grenoble. He was in the electronics lab of the French Atomic Energy Commission for six years and then worked in signal processing for an industrial firm before joining HP France in late 1974. He wrote most of the 3070B firmware and contributed to the multifunction reader and the terminal's electronics. Married, and with two children, Daniel spends his spare time gardening and is also kept busy as a member of the city council in his local community, Brié et Angonnes, a residential community near Grenoble.

SPECIFICATIONS

HP Model 3070B Terminal

DISPLAY: 15 position (written left to right).
DISPLAY CHARACTER SET: 0 through 9, decimal point, space, E, □ (used to indicate a special function key has been depressed).
CHARACTER GENERATION: 7-segment LED (red).
CHARACTER SIZE: 4.0 mm (enhanced by magnification).
PROMPTING LIGHTS: 15 red LEDs.
POWER-ON INDICATOR: Green LED.
WAIT INDICATOR: Red LED.
KEYBOARD: Buffered, N key roll over. Numerals 0 through 9, decimal point, minus, **Enter** and **Delete**. Ten special function keys (may be programmed to be tagged with a terminator character). Gold attention key (sets HP-IB SRQ line when depressed).
CONTROLS (at rear of instrument): Power ON/OFF, voltage selector, self test.
AUDIBLE ALARM: Internal buzzer sounds on receipt of Bell character or invalid use of terminal.
PROGRAMMING: Keyboard and/or display may be configured or deconfigured by transmitted command.
HP-IB KEYBOARD/DISPLAY ADDRESS: Factory set at 35 octal; modifiable by switch.

Communications

SERIAL LINK:
CABLE: Shielded twisted pair.
SIGNAL LEVELS: 5 volts, differential; isolated through optical couplers.
DISTANCE: Total length of link cable may be up to 4 km. Computer and terminals can be connected randomly at any point on the link providing no terminal is more than 2 km from the computer.
TRANSMISSION SPEEDS: Link operates at 25k bits/second; effective data transfer rate depends upon number of terminals connected and varies between 12 transfers/second/terminal (63 terminals) to 280 transfers/second/terminal (1 terminal).
TERMINAL ADDRESS: Selectable from 1 to 63 by rear-panel switch.
COMPUTER INTERFACE: For each data collection system (up to 63 terminals*), one 40280A Interface Card is needed to interface HP 21MX-Series Computers to serial-link cable.
*Maximum of 56 with HP System 1000.

HP-IB:
SIGNAL LEVELS: All lines ground true. 1 = ≤0.8V (low state), 0 = false ≥2.0V (high state).
LOADING: 2 HP-IB loads.

Printer

TYPE: Thermal, 5.7 cm wide paper roll (2.25 inches).
SPEED: 50 lines per minute. Transmitted data is buffered before printing. BUFFER: 40 characters.
FORMAT: 7 × 5 dot matrix, 20 characters per line.
CHARACTERS: 64 ASCII character set.
CONTROLS: Print ON/OFF switch; manual paper advance.
PROGRAMMING: Printer on/off may be configured by transmitted command. End of paper status.
HP-IB ADDRESS: Automatically set at keyboard/display address minus 2 (i.e. factory set at 33 octal).

Multifunction Reader

ACCEPTS:
Perforated plastic badges nonembossed (industry type III) from 1 up to 22 columns of alphanumeric data. Badge size: 8.26 × 5.9 cm (3.25 × 2.3 in.).
Standard 80-column punched cards.
Variable column density (up to 80 col) punched cards with clock marks printed. Card size: 8.26 × (5 to 40 cm) (3.25 to (2 to 16) in.).
Optical mark forms of fixed 40-column density without clock marks.
Optical mark forms of variable column density (up to 80 columns) with clock marks printed. Form size: 8.26 × (5 to 40) cm 3.25 to (2 to 16) in.).
READING RATE: Up to 1 badge or form per second. Data is buffered before data transmission. Buffer size: one form (up to 160 characters).
HP-IB ADDRESS: Automatically set at keyboard/display address minus 1 (i.e. factory set at 34 octal).

PROGRAMMING: Reader may be configured or deconfigured by transmitted command. Reading mode defined by:
Clock/no clock marks.
Clock on/clock after data mark position.
ASCII/Image reading mode.
40-column/80-column fixed density.
Punched holes/holes and marks.
Local card entering error detection enabled/disabled.
Known preset configuration may be obtained at power on by use of switches.

General

ENVIRONMENTAL
TEMPERATURE: Free space ambient. Operating, 0° to +55°C. Nonoperating, −40° to +70°C.
HUMIDITY: 5% to 95% (noncondensing).
HEAT DISSIPATION: 25 watts maximum.
VIBRATION AND SHOCK: Type tested to quality for normal shipping and handling.
FORMS: Reader is designed to read forms that meet specifications over 20% - 75% RH range at 23° C (73° C), and in most cases will work beyond this range.
BADGES: Dimensions of badges should be within following specifications from 0° to +55° C.:
LENGTH: 82.6 mm (3.25 in.).
WIDTH: 59.1 mm (2.3 in.).
THICKNESS: 0.8 mm (0.03 inches) maximum, 0.3 mm (0.012 in.) minimum.
HOLES: size and position confirm to ANSI spec 3-11-1969.
POWER: 115V (+10%, −25%), 230V (+10%, −15%), 47.5–66 Hz, 50 watts maximum. UL approved, CSA and VDE approvals pending.
DIMENSIONS: 157 mm H × 277 mm W × 400 mm D (6.2 × 10.9 × 15.7 in.).
WEIGHT: 5.9 kg (13 lbs.).
PRICE IN U.S.A.: Model 3070B, $3200. 40280A Interface Card, $1200.
MANUFACTURING DIVISION: HEWLETT-PACKARD FRANCE S.A.
5 Avenue Raymond Chanas
F-38320, Eybens (Grenoble)
France

Hewlett-Packard Company, 1501 Page Mill Road, Palo Alto, California 94304

HEWLETT-PACKARD JOURNAL

JULY 1978 Volume 29 • Number 11

Technical Information from the Laboratories of Hewlett-Packard Company

Hewlett-Packard Company, 1501 Page Mill Road
Palo Alto, California 94304 U.S.A.
Hewlett-Packard Central Mailing Department
Van Heuven Goedhartlaan 121
Amstelveen-1134 The Netherlands
Yokogawa-Hewlett-Packard Ltd., Suginami-Ku
Tokyo 168 Japan

Editorial Director • Howard L. Roberts
Managing Editor • Richard P. Dolan
Art Director, Photographer • Arvid A. Danielson
Illustrator • Susan E. Wright
Administrative Services, Typography • Anne S. LoPresti
European Production Manager • Dick Leeksma

Bulk Rate
U.S. Postage
Paid
Hewlett-Packard
Company

CHANGE OF ADDRESS: To change your address or delete your name from our mailing list please send us your old address label (it peels off). Send changes to Hewlett-Packard Journal, 1501 Page Mill Road, Palo Alto, California 94304 U.S.A. Allow 60 days.