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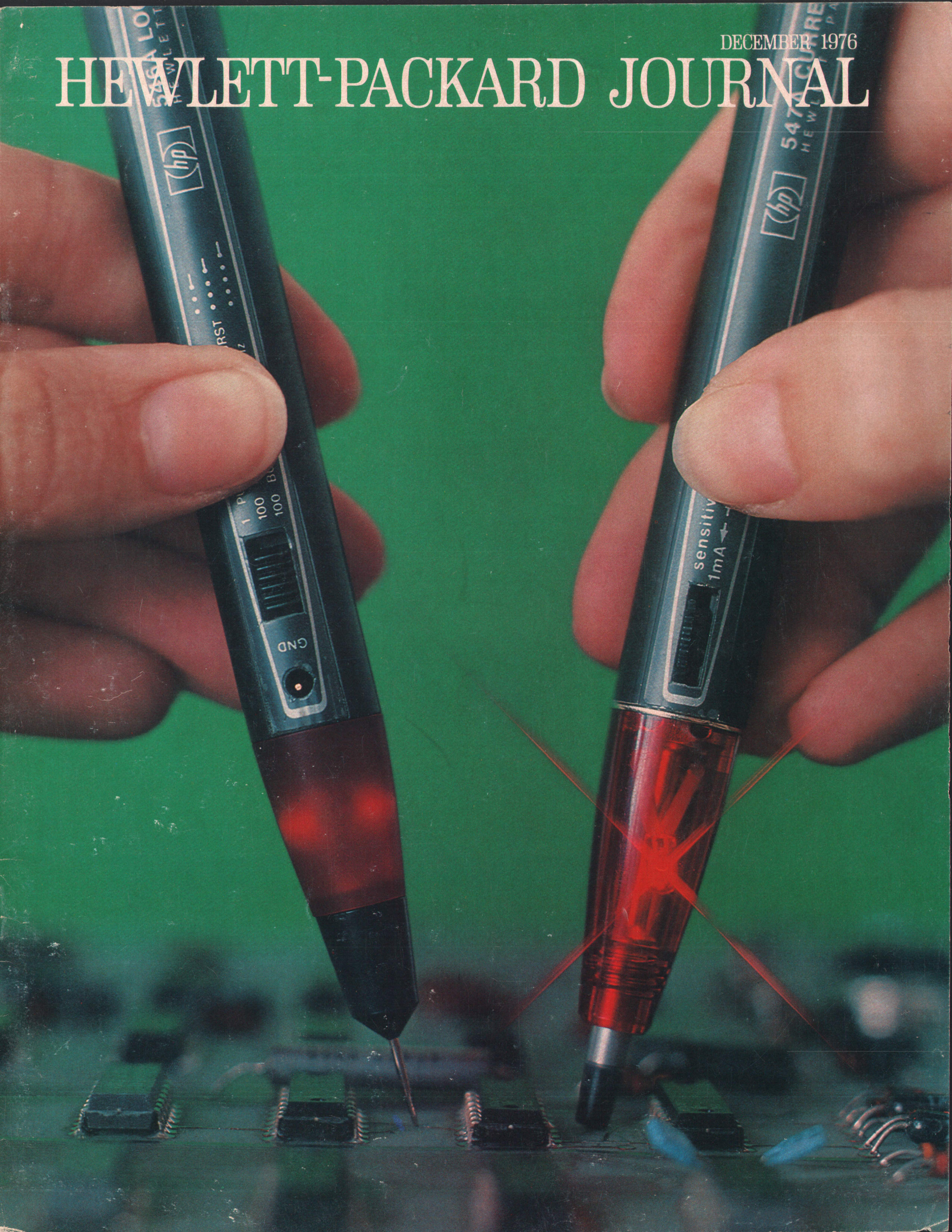


# Current Tracer: A New Way to Find Low-Impedance Logic-Circuit Faults

*By tracing current pulses, this sensitive probe helps locate solder bridges, shorted conductors in cables, shorts in voltage distribution networks, shorted IC inputs and dead or stuck outputs, stuck wired-AND circuits, and stuck data buses.*

**by John F. Beckwith**

FOR TROUBLESHOOTING DIGITAL systems, instruments such as logic probes, logic pulsers, logic comparators, state analyzers, and computer-based board testers enable an operator to localize a system malfunction down to the faulty node, that is, down to a collection of IC terminals and the network of printed circuit traces and/or wires that electrically tie the terminals together. However, after the faulty node is identified the operator still lacks the ultimate information needed to make the repair, namely, exactly what part of the node has failed? Is the driving IC dead, or has one of the driven ICs developed a shorted input? Has the interconnecting network shorted to another node, and if so, precisely where, or has the interconnecting network developed an open circuit? Except when the fault is due to an open circuit, voltage-sensing instruments provide no further information, simply because all points of the faulty node are constrained by the interconnecting network to be at the same voltage. At this stage, techniques such as cutting traces or lifting ICs are usually employed until the defective element is identified. This approach is time-consuming, tedious, and often damaging to the printed circuit board and ICs.

Although voltage provides no additional information, there is a quantity whose variation about the node provides the information needed to pinpoint the faulty element. This quantity is current. To date, little use has been made of the information provided by the nodal current distribution simply because of the difficulty of measuring current flow. Traditional methods, such as cutting a trace and inserting an ammeter, or encircling the trace with a magnetic path, are clearly very awkward to use on printed circuit boards. The question thus arises whether there is a more convenient means to determine current flow in logic circuits.

The new Hewlett-Packard Model 547A Current Tracer (Fig. 1) was developed to meet this need. The current tracer is a self-contained, hand-held probe containing a single easily-viewed display lamp whose intensity indicates the relative magnitude of current steps occurring in the vicinity of the current tracer's tip. The reference level for the display can be varied from one milliampere to one ampere by means of a conveniently placed sensitivity control. The 547A responds to the current changes normally pre-

**Cover:** *A new troubleshooting team finds many low-impedance faults that elude voltage-sensing instruments. Model 547A Current Tracer (right) reveals the presence and relative size of current steps by the brightness of its built-in lamp. Model 546A Logic Pulser supplies the needed stimulus current if it isn't already present in the system under test.*

**In this Issue:**




**Fig. 1.** *The lamp near the tip of the new Model 547A Current Tracer varies in brightness according to the relative magnitude of the current steps occurring near its tip. By observing how the lamp's brightness changes as the tracer is moved along the conductors the user can follow the flow of current.*

sent in digital circuits and typically does not require the injection of a stimulating signal. When a stimulus is required it may be provided by a logic pulser such as the HP Models 546A or 10526T. Synchronizing signals between pulser and current tracer are not needed. The 547A is compatible with all logic families including CMOS. It responds only to current and possesses sufficient sensitivity and dynamic range to detect currents resulting from faults in any of the presently available families. Power for the current tracer may be derived from any dc source between 4.5 and 18 volts. No ground reference is required and a floating battery may be used if desired.

To operate the current tracer the user first places its tip near the driving point of the node, which is usually one of the IC terminals, or near the tip of the logic pulser when the node needs an external stimulus. Then the sensitivity control of the current tracer is adjusted until the display lamp is between one-half and fully lit. At this point the operator can get an indication of the magnitude of the current flowing simply by noting the position of the sensitivity control. This information is often very useful in determining the nature of the fault. For example, if the current tracer indicates an abnormally high current, then the fault is due to a low impedance. The operator then moves the tip of the tracer along the conductive paths, and by noting the intensity of the indicator lamp, can tell if current is present near the tip. In this manner, he can follow the current directly to the fault. The current tracer's tip need not make physical contact with the conductive path, so current can be followed in insulated wires and along inner traces of multilayer boards.

### The Current Tracer in Use

Fault localization in digital systems is the major applications area for the current tracer, but there are others as well. Whenever a low-impedance fault exists, whether on a digital board or not, the shorted node can be stimulated with a logic pulser and the current followed by means of the current tracer. Some typical current tracer applications are described in the paragraphs that follow.

- **Ground planes.** An interesting application of the current tracer is designing ground planes and determining their effectiveness by tracing current distribution through the plane. Current is injected into the ground plane using either a logic pulser or a pulse generator, and current flow is easily traced over the plane. Often the results are surprising in

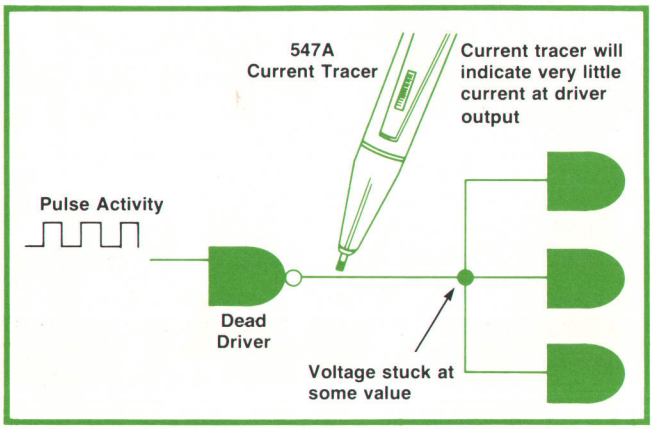



**Fig. 2.** *Using the current tracer to determine that a stuck node is caused by a dead driver.*

that current flows through only a few paths, or along edges.

- **$V_{cc}$-to-ground shorts.** Locating $V_{cc}$-to-ground shorts is an almost impossible task without the ability to trace current flow. To find the short, the user disconnects the power supply and pulses the power supply terminal using the logic pulser with the supply return connected to the GND lead of the pulser. Even if capacitors are connected between $V_{cc}$ and ground, the current tracer will usually reveal the path carrying the greatest current.
- **Stuck node caused by dead driver.** Fig. 2 illustrates a frequently occurring troubleshooting symptom: a node has been identified on which the voltage is stuck high or low. Is the driver dead, or is something, such as a shorted input, clamping the node to a fixed value? This question is readily answered by tracing current from the driver to other elements on the node. If the driver is dead, the only current indicated by the tracer will be that caused by parasitic coupling from any nearby currents, and this will be much smaller than the normal current capability of the driver. On the other hand, if the driver is good, normal short circuit current will be present and can be traced to the circuit element clamping the node.
- **Stuck node caused by input short.** Fig. 3 illustrates this situation, which has exactly the same voltage symptoms as the previous case of a stuck node caused by a dead driver. However, the current tracer will now indicate a large current flowing from the driver, and will also make it possible to follow this current to the cause of the problem, the shorted input. The same procedure will also find the fault when the short is on the interconnecting path of the node—for example, a solder bridge to another node.

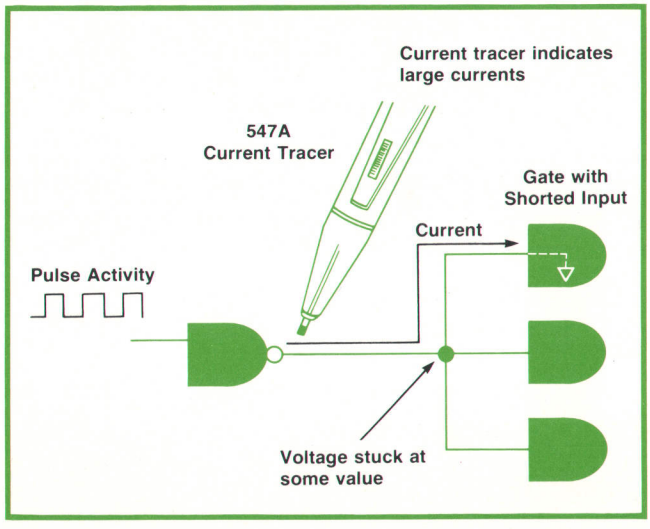



**Fig. 3.** *The current tracer shows that this stuck node is caused by an input short.*

- **Stuck wired-AND node.** Another difficult circuit problem to troubleshoot is the wired-AND node, a node formed by connecting several open-collector output structures. Fig. 4 shows how the current tracer is used to solve this problem. Each gate's output is placed in turn in its off or high-impedance state by forcing the inputs to an appropriate level (a jumper may be used) while a logic pulser is used to stimulate the output node. If the gate is good the current tracer will indicate only stray current at the gate output. Conversely, a stuck gate will result in a large current indication. The need to force the output of the gate to the off state by means of the jumper at the input can be eliminated if the duty cycle of the high-impedance state when the circuit is operating is not too low. When this is the case a logic pulser and current tracer may be used in the single-pulse mode. If the gate is not stuck the operator should observe a random presence and absence of current at the gate output while single-pulsing the node. If the gate is stuck, each pulse from the pulser will result in a large current indication from the tracer.
- **Stuck three-state data bus.** A stuck three-state bus, such as a microprocessor data or address bus, pre-

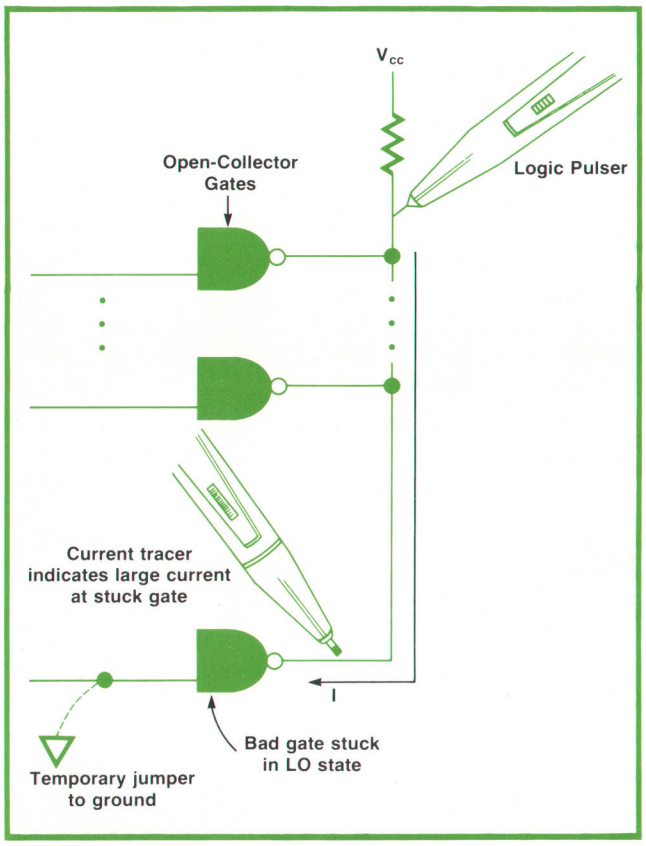



**Fig. 4.** *The current tracer can often make use of normal currents in a circuit, but sometimes a logic pulser provides a needed stimulus, as in the difficult problem of a stuck wired-AND node.*

sents a very difficult troubleshooting problem, especially to voltage-sensing measurement tools. Because of the many bus terminals, it is very difficult to isolate the one bus element holding it in a stuck condition. However, if the current tracer indicates high current at several driver outputs, it is likely that one (and most likely *only* one) driver is stuck in a low-impedance state. The defective driver is located by placing one driver's control input line to the appropriate level for a high-impedance output state and noting whether high current flow persists at the output. This is repeated for each driver until the bad one is located. Alternatively, if the low-impedance duty cycle of a driver is low, the node can be pulsed with the logic pulser, and the defective driver identified by noting whether every pulse from the pulser results in current at the driver output. If the current tracer indicates high currents at only two drivers the problem is a "bus fight", that is, both drivers trying to drive the bus at the same time. This is probably caused by improper control signals to the drivers. If the current tracer indicates the absence of abnormally high current activity at all drivers, yet the bus signals are known to be incorrect, then the problem is a driver stuck in the high-impedance state. It can be found by placing a low impedance on the bus, such as a short to ground, and using the current tracer to check for the driver that fails to show high-current activity.

Efficient use of the current tracer usually requires a longer familiarization period than does the operation of voltage-sensing instruments. This is primarily because most operators are not used to thinking in terms of current and the information it provides, simply because this information has not been available conveniently. Also, it requires some skill to avoid the crosstalk problem, that is, if a small current is being traced in a conductor that is very close to another conductor carrying a much larger current, the sensor at the tip of the current tracer may respond to the current in the nearby trace. The current sensor has been designed to minimize this effect, but it can never be entirely eliminated. The operator can, however, by observing the variation of the current tracer's display as its tip is moved about the trace, learn to recognize interference or crosstalk from a nearby trace.

### Inside the Current Tracer

Fig. 5 is a block diagram of the current tracer. Operation is as follows. A step change in current occurring at the current tracer's tip is coupled via mutual inductance to the current-step sensor, which produces a voltage impulse output proportional to the magnitude of the current step. The size of the impulse decreases with increasing separation between the current path and the tip of the tracer.

The voltage impulse is fed to a variable-gain preamplifier. The preamplifier gain is adjusted by the sensitivity control to produce an output of approximately 1 mV when the tracer's tip is placed next to the current path. The output of the preamplifier is further amplified and then stretched by two cascaded peak detectors to produce a pulse of sufficient height and width to cause a visible flash of the incandescent lamp that forms the current tracer's display. When the tip of the tracer is moved along the conducting path the display remains at the same brightness as long as the same current is still present. However, if the current has changed to another path, the increased separation between the tip of the tracer and the current lowers the output of the current-step sensor and decreases the brightness of the display. Thus the operator is provided with sufficient information to track the current path.

### Current-Step Sensor

Fig. 6 shows the physical construction and an equivalent circuit of the current-step sensor. Its operating principle is essentially that of a current transformer. A step change in current near the tip of the tracer attempts to induce an emf in the windings on the coil within the sensor. This coil is nearly shorted

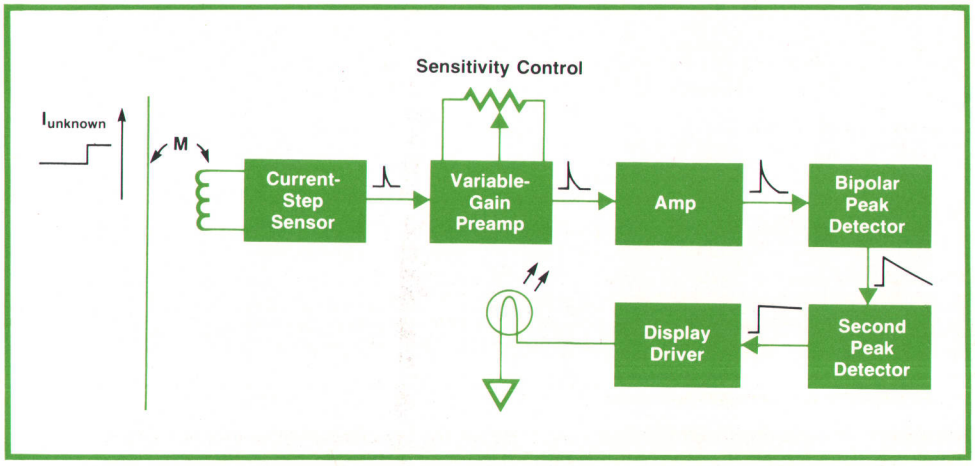



**Fig. 5.** *547A Current Tracer block diagram. Current-step sensor detects current steps as small as 1mA and rejects magnetic flux that is not directly beneath the tracer's tip.*

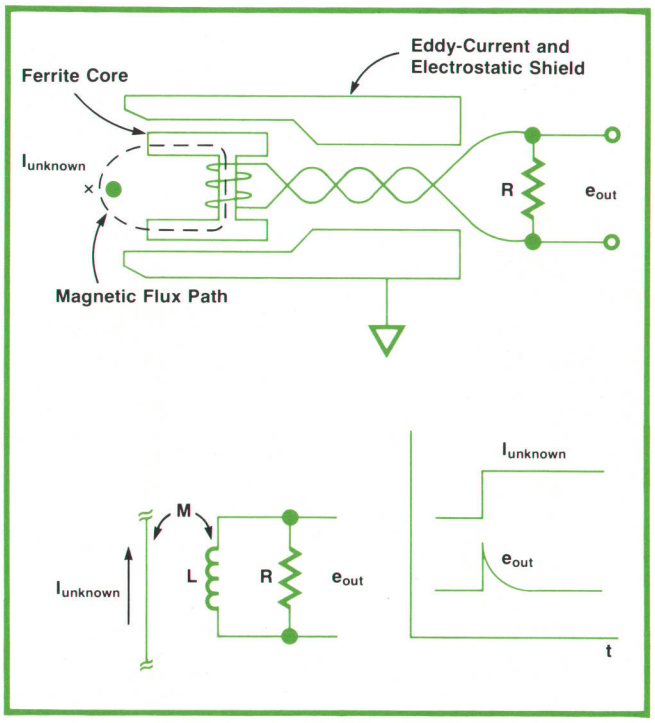



**Fig. 6.** *Construction and equivalent circuit of the current-step sensor, which acts like a current transformer. For each current step the sensor produces a voltage impulse at its output.*

(R is small), so a current is induced in the coil whose magnetic flux nearly cancels the flux change caused by the unknown current step. Thus, for a fixed physical orientation, there will be a current step proportional to the unknown current step induced in the pickup coil. This induced current flows through the resistor R, producing a voltage that forms the output signal of the sensor. The current in the pickup coil, and hence the output voltage, decays with a time constant L/R. This time constant is such that the output of the current-step sensor is an impulse whose peak value is proportional to the change in the unknown current and is independent of the rise time of the current change up to about 200 nanoseconds. Although the current-step sensor provides an indication only of current changes and not the total value of the current, it turns out that for fault finding in digital systems this information is sufficient.

The current-step sensor had to meet a number of conflicting design criteria. It had to be physically small so currents in the closely spaced traces found on printed circuit boards could be distinguished. It had to be able to reject magnetic flux originating from locations other than the tracer's tip. It had to provide a detectable output for the smallest current steps of interest (<1 mA). It could not respond to voltage changes found in digital systems. It had to be mechanically rugged and manufacturable at a reasonable cost.

These criteria were successfully met by enclosing a very small (1.5-mm-diameter) H-shaped ferrite core within a relatively thick, highly conductive shield. The shield serves several purposes: it provides mechanical support and protection for the pickup core, it shields the core from external changing magnetic fields by means of induced eddy currents in the shield that oppose the changing flux, and it is electrically grounded and thus protects the coil windings from electric fields caused by the voltages on the board. Protection from electric fields is adequate to provide the greater than 110 dB of shielding needed so the tracer's tip can be placed next to voltage steps of five volts and not respond to them, while at the same time responding to current steps of 1 mA. For a 1-mA current step the current-step sensor produces a 100-$\mu$V output spike approximately 150 ns wide.

### Amplification

To make a 100-$\mu$V 150-ns pulse light an incandescent lamp long enough for it to be visible, considerable amplification is required. For the sake of operating convenience, it was decided to package all the necessary electronics in the probe body and to power the probe from the supplies typically present in a digital environment. This means that the circuitry has to operate from supply voltages of five volts or less, so nearly all commercially available linear ICs are inapplicable. Also, the shape and small size of the probe body make physical isolation of the amplifier stages impractical, and the small volume within the probe also prevents the use of effective high-frequency decoupling capacitors because of their large size. It was possible, nevertheless, using two custom ICs, to package on a multilayer board approximately 1.3 cm wide by 10 cm long, 80 dB $\times$ 20 MHz of stable linear amplification. This was accomplished by very careful location of components to minimize capacitive coupling, and by orienting the components to cancel destabilizing parasitic inductive coupling. Shielding of the sensitive amplifier from external electric and magnetic fields is provided by the probe housing, which is made of aluminum and makes an effective electrostatic and eddy-current shield.

For maximum viewing angle, brightness, and convenience of location, the current tracer's display was chosen to be an incandescent lamp at the tip of the probe immediately behind the current-step sensor. This location creates a difficult stability problem: a pulse at the current-step sensor is amplified and returned to the display, which is right next to the sensor, and the energy content of the pulse that flashes the display can be greater than $10^{14}$ times that captured by the current-step sensor. It was possible, however, thanks to the efficiency of the shielding of the

current-step sensor, the orientation of the amplifier components, and careful printed circuit board design to electrically decouple the input from the output. In fact, the current pulse that drives the display lamp actually passes through the board area in which the amplifier is located, but by running the display lamp's supply and return traces on the inner layers of a multilayer board, one above the other and separated by a very thin insulating layer, and covering these with the outer-layer ground plane, it was possible to confine the fields from the display pulse to a very small volume. The ground plane also had to be carefully designed so the charging currents of the parasitic capacitor formed by the grounded eddy-current shield and the trace or node under investigation can pass through the sensitive amplifier area without inductively coupling unwanted signals to the amplifier.

Fault currents in the various logic families and from pulse stimulators can vary from about one milliampere to one ampere. The tracer normalizes these to a common reference level so the operator sees only the value of the current at the tracer's tip relative to that at the driving point of the node. This 60-dB (1000:1) gain variation cannot be achieved with a potentiometer divider because the parasitic inductances and capacitances associated with a potentiometer at the extreme positions of the wiper degrade the high-frequency response. Also, the gain control has to be in the initial stages of the amplifier chain because the requirement of operating from five-volt supplies severely restricts the linear operating range of the amplifiers. For these reasons the entire 60 dB of gain control was placed in the first amplifier stage. This was done by taking as the basic configuration a single transistor with an unbypassed emitter resistor approximately equal to the collector resistor (see Fig. 7). Current-controlled variable resistors formed from Schottky and silicon diodes are ac-coupled to both the collector and emitter resistors. When the sensitivity control on the tracer is placed in the 1-mA position the variable emitter resistors are in their low-resistance state and the collector resistances are in their high-resistance state, thus forming a common-emitter amplifier of 20-dB gain. Conversely, when the sensitivity control is in the 1A position the collector resistance becomes very small and the emitter resistance large and the configuration forms a 40-dB attenuator. A temperature-compensated, precision-component network was required to provide control currents for the variable resistors to insure that the maximum and minimum values of the amplifier gain were repeatable from unit to unit and stable with time.

The noise performance required of the first amplifier stage is quite severe. It must amplify, with a 20-MHz bandwidth, input pulses smaller than 100 microvolts and yet not introduce any noise peaks comparable in amplitude to the input pulses because the downstream circuitry detects each peak and stretches it for a sufficient time to light the display. Thus the rms noise introduced by the amplifier must be far below the 100-microvolt input pulse. This was achieved by using a low-noise, high-frequency transistor biased to optimize its noise figure.

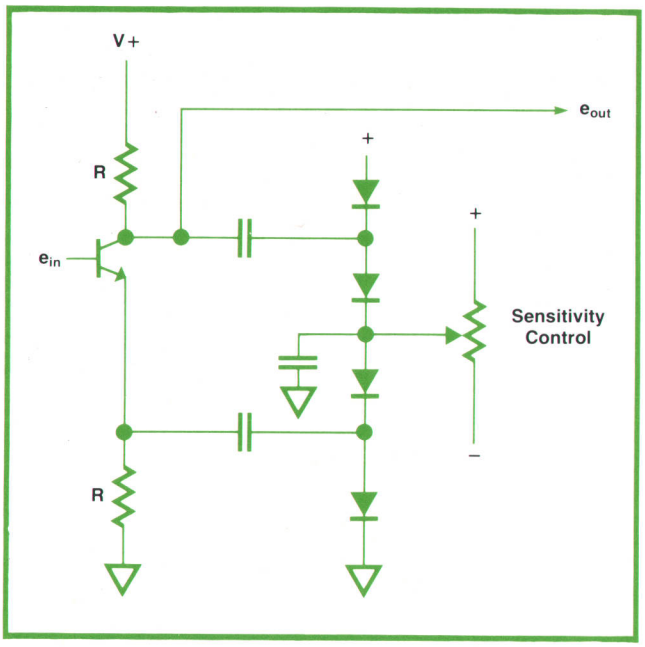



**Fig. 7.** *Variable gain preamplifier provides 60 dB of gain variation as the sensitivity control is adjusted. The diodes function as current-controlled variable resistors.*

### Peak Detectors

When the sensitivity control is set so the display is at its reference level, the output of the current-step sensor emerges from the amplifier chain with an amplitude of about 500 mV and a width of about 150 nanoseconds. The polarity of this output will be either positive or negative, depending upon the polarity of the current step and the randomly chosen orientation between the current path and the pickup coil in the tracer. The operator is interested only in how the magnitude of this pulse varies as he moves the tip of the tracer from place to place, so the signal that drives the display lamp must be proportional to the amplitude of the output of the amplifier chain, independent of its polarity, and of sufficient duration to be visible. The required signal processing is accomplished by means of two peak detectors. The first, or bipolar peak detector (Fig. 8), produces an output pulse of the same magnitude as the input pulse, but always of the same polarity, and stretches the peak of the input pulse from about 20 ns to about 40 $\mu$s. A second peak detector stretches the output of the bipolar peak detector to about 200 ms, which is long enough to be vis-

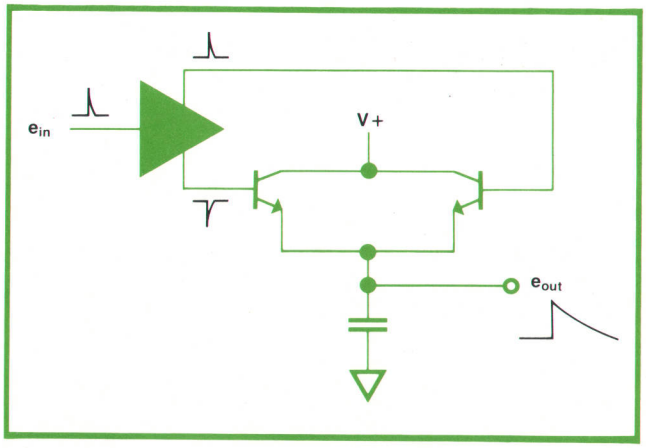



**Fig. 8.** *The output of the bipolar peak detector is a time-stretched version of the input, and is positive for both polarities of input.*

ible. The output of the second peak detector is further amplified by a dc amplifier to provide the signal that lights the incandescent display lamp.

### Voltage Regulator

The current tracer is designed to operate from any external dc supply between 4.5 and 18 volts and to withstand accidental reversals of supply voltage polarity. The internal tracer supply voltage is independent of the magnitude of the external supply voltage. It is obtained by a feedback configuration using a special PNP series-pass transistor that has a very high emitter-base breakdown voltage to assure reverse-polarity protection (see Fig. 9). The value of the internal supply voltage is set by the balancing of a "nonlinear bootstrap bridge", a bridge containing a diode in one arm and driven by the internal supply itself. Because of the nonlinearity of the diode only one value of the internal supply voltage will balance the bridge. Any unbalance is amplified and negatively fed back to the series-pass transistor to complete the loop. This configuration permits nearly all of the external supply voltage to be used when the external voltage is low.

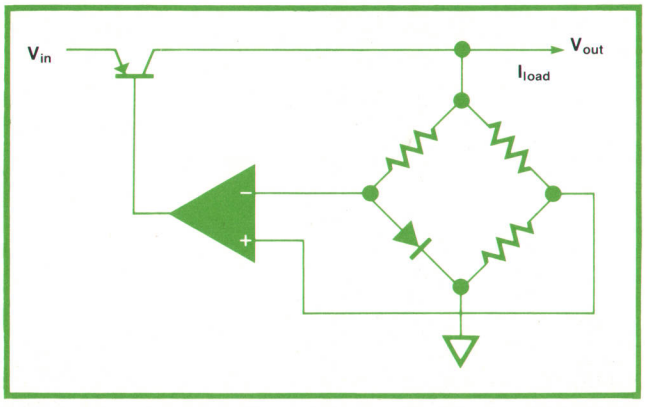
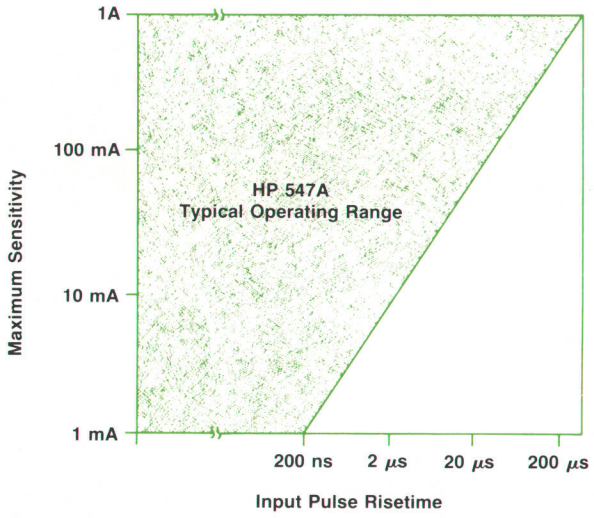



**Fig. 9.** *Voltage regulator output voltage is constant regardless of load current and input voltage as long as the input voltage exceeds the regulated output voltage by as little as the saturation voltage of the transistor.*

## SPECIFICATIONS
### HP Model 547A Current Tracer

**INPUT:**
SENSITIVITY: 1 mA to 1A
FREQUENCY RESPONSE: Light indicates: single-step current transitions; single pulses ≥50 ns in width; pulse trains to 10 MHz (typically 20 MHz for current pulses ≥10 mA).
RISETIME: Light indicates current transitions with risetimes ≤200 ns at 1 mA.
**POWER SUPPLY REQUIREMENTS:**
VOLTAGE: 4.5 to 18 Vdc
INPUT CURRENT: ≤75 mA
OVERVOLTAGE PROTECTION: ±25 Vdc for one minute
**TEMPERATURE:** 0° to 55°C
**PRICE IN U.S.A.:** $350
**MANUFACTURING DIVISION:** SANTA CLARA DIVISION
5301 Stevens Creek Boulevard
Santa Clara, California 95050 U.S.A.




**John F. Beckwith**

John Beckwith received his BSEE degree in 1959 from Georgia Institute of Technology, and his MS degree in physics in 1967 from Florida State University. Before coming to HP in 1973, he designed several commercial products, mainly computer terminals, gathering experience in digital, analog, broadband-linear, magnetic, and electromechanical design. He also spent two years in business for himself, developing an inventory control system. At HP, besides designing the 547A Current Tracer, he's helped design a laser calibrator and an RF signal generator. John was born in New York City and raised in Florida. He's married, has two children, lives in Foster City, California, and likes to work on cars. He's also a student of economics, government, and law, and occasionally takes an active part in local government. Quantum electrodynamics is another of his continuing interests.

# New Logic Probe Troubleshoots Many Logic Families

*The probe's single lamp indicator displays high or low logic levels, bad levels, and open circuits on digital circuit nodes. Testable logic families include TTL, DTL, CMOS, HTL, HNIL, and MOS.*

**by Robert C. Quenelle**

DESIGNING AND TROUBLESHOOTING digital circuits poses some measurement problems not neatly solved by analog test equipment. The digital circuit typically has only two narrow voltage ranges, high and low, that represent logic ones and zeros. A voltmeter or oscilloscope will easily give the voltage to more accuracy than is required, but won't translate those voltages into logic levels, leaving that job to the user. Although the oscilloscope is sometimes indispensable for checking ringing, skews, and so forth, in many instances a simple indication of logic levels will suffice.

For several years the logic probe has complemented the oscilloscope in helping to solve digital troubleshooting problems. HP's Model 10525T, for example, is small and light enough to be hand-held and features convenient fingertip display of ones and zeros and 10-nanosecond pulse-catching capability, independent of repetition rate. The 10525T translates voltages at the measurement tip to logic levels based on the specifications of TTL logic.

With the expanding use of MOS and CMOS, it became desirable to have more than TTL thresholds available. The new HP Model 545A CMOS-TTL Logic Probe (Fig. 1) offers switch-selectable TTL or CMOS thresholds for monitoring acitivity in most logic families, including DTL, TTL, HTL, HNIL, MOS, CMOS and discrete logic (but not ECL). The CMOS thresholds are set at 30% and 70% of the supply voltage to which the 545A is connected.

Most MOS parts are either TTL-compatible or have logic levels close to some power supply voltages. By selecting TTL thresholds for TTL-compatible parts or by using CMOS thresholds and connecting the probe to appropriate supply voltages, most MOS devices can be checked. The probe always displays the more negative logic level as a zero. HTL or HNIL parts are tested using CMOS thresholds. The input current is nominally 10 $\mu$A (source and sink), compatible with high-impedance logic yet large enough to overcome leakage currents and prevent false readings. Besides displaying ones and zeros, the probe indicates voltages between valid logic levels, as well as open circuits or inputs not connected to outputs.

The probe contains a latch that indicates and stores input activity, a useful feature when low repetition


**Fig. 1.** *Model 545A Logic Probe indicates logic levels and pulse activity at individual digital circuit nodes.*

## A Smart Probe-Test System

Instrument test procedures can have substantial effects on factory cost, warranty cost, and customer satisfaction. High-volume, high-technology instruments like the new logic products demand high test throughput and a high test confidence factor, the latter because warranty cost on a returned low-cost instrument represents a large portion of its price.

The solution was found in a calculator-controlled test system. The system is a closed-loop, self-calibrating, fully automatic tester. Most of the hardware is off-the-shelf instrumentation: an HP 9830A Calculator as system controller, an HP 9866A Printer for failure analysis and statistical data, an HP 5328A Counter with built-in DVM for dc voltage measurements and a programmable input section for dynamic pulse measurements, an HP 59303A DAC to program the voltage on an HP 6824A Power Amplifier, another DAC to program dc probe tip voltages, an HP 1900 Pulse Generator System to provide dc and dynamic signals, an HP 59301A HP-IB-to-Parallel Converter to program the instrument interface test boxes and the 1900 Pulse Generator ranges, another 59301A to program an 8-channel 6-bit DAC to set the verniers on the pulse generators, and two HP 59307A VHF Switches to route the VHF signals going between the generators, the two instrument interface test boxes, and the counter. The counter is also used to close the loop back to the calculator under software control for accurately setting the dc and dynamic stimulus circuitry. The counter's DVM port is used to get test-box control signals into the calculator. The 5328A Counter is the only part of the system requiring periodic off-line calibration. Everything else can be recalibrated automatically with correction factors stored in a software calibration file.

Inside the two identical instrument interface test boxes are solenoids that push buttons and slide switches, microswitches that sense whether a probe, pulser, or current tracer is plugged in, phototransistors and amplifiers to measure the brightness of indicators, VHF relays for pulse line termination and load sensing, reed relays for direct voltage measurement, and support electronics.

In operation, all the operator need do is load the operating system tape cassette into the calculator, plug a probe or pulser into the left hole of either test box or a current tracer into the right hole, and press the test button. The system selects the box, identifies which instrument is plugged in, runs the proper test program, lights the pass or fail lamp upon completion of the test, and if the instrument fails, prints out a failure analysis and diagnostic message helpful in repairing the instrument.

*-Barry Bronson*

rates or single-shot events are involved. A light-emitting diode (LED) indicator turns on when a new one or zero level is detected and stays on until manually reset.

To protect the 545A from accidental overloads, the power supply input is protected to ±25 volts for one minute and the tip can withstand momentary overloads to 250 volts. The probe is usable down to three volts, although the tip lamp gets dimmer below five volts. CMOS supplies often have considerable ripple, especially if electrically noisy devices use the same supply. In the CMOS mode the probe's thresholds track the instantaneous supply voltage as does CMOS logic, thereby compensating for ripple to 1 kHz.

### Using the Probe

The logic probe has two main display modes, static and dynamic. It indicates in a static circuit whether the voltage at a particular point is a logic zero, a one, or an indeterminate level. The lamp in the probe tip is off for a zero, bright for a one, and dim for a voltage between logic levels, an open circuit, or a high-impedance point such as a floating input or a three-state output in the off state. In a dynamic circuit, the tip lamp will flash at about 10 Hz when the tip is touched to a point toggling between a one and zero at up to 80 MHz in TTL mode and 40 MHz in CMOS. It will flash on or off for about 50 ms for a single one or zero pulse. Pulses as short as 10 ns can be detected if the short ground lead is connected to a point near the pulse source. 20-ns pulses can typically be detected without using the short ground lead. The probe can also be clipped into a circuit and the latch used to monitor infrequent activity.

By displaying the dc logic levels in a circuit the logic probe can be used to verify combinatorial relationships. Or, input levels can be overridden by a logic pulser and the logic probe will then test the functioning of a circuit without removing any normal connections. In clocked systems, many logic families respond only to clock transitions and are insensitive to the clock rate (up to their upper frequency specifications). This allows replacing normal clocking signals with a single cycle or slow clock (once again, a logic pulser may be used) and checking system sequencing at a convenient rate. Spikes and one-shot outputs can also be checked even at slow clock rates

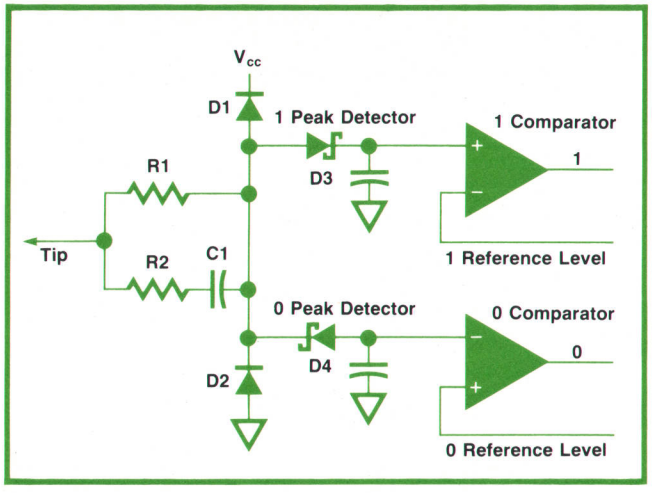



**Fig. 2.** *545A front-end has two fast peak detectors and two relatively slow, low-input-current comparators. The circuit can withstand accidental overloads of ±120V continuous and ±250V for 15 seconds.*

because of the 545's pulse stretching display.

The 545's dynamic capability allows checking circuits running at full clock rate. Dead nodes (stuck high, low, or bad-level/open) are common failures easily found with the probe. Spikes on normally quiet lines (such as reset) will also show up even if the duty cycle is very low. Often a technique similar to analog signal tracing can be used to find problems. Working back from an output to a point where a gate's inputs are moving but the output is not will localize many faults.

### Inside the Probe

The heart of the 545A Logic Probe is a custom HP integrated circuit containing input comparators, reference circuits, logic for controlling the tip lamp and latch LED, timing circuits, and a lamp driver for operating the lamp over a 3-to-18-volt power supply range. The input signal is connected to two comparators through peak detectors and an external RC network (see Fig. 2). The peak detectors use Schottky diodes (D3 and D4) for fast switching and make it possible to use relatively slow, low-input-current comparators. Protection from input overloads is provided by on-chip clamp diodes (D1 and D2) and the external network. R1, the dc path, allows signals up to 250 volts to be momentarily applied while R2 and C1 provide a damped bypass for fast pulses.

The logic section operates asynchronously, triggered by data changes at the input. The internal state, indicated by the tip lamp, and the input history since the last display change determine the next state. A new zero or one signal starts a cycle that updates the display, then waits 50 ms to produce a stretching or toggling effect. The new zero or one signal also sets the memory indicator, which stays on until manually reset. If neither a zero nor a one is present and the timing cycle is complete, the logic displays a bad level (dim lamp) until a valid logic level arrives.

To provide power supply overvoltage and reversal protection and the ability to operate at three volts, it was necessary to provide a protection circuit with low voltage drop. In Fig. 3, Q1 is a series-pass transistor that remains saturated in normal operation. The FET, Q2, provides base drive for Q1 that is relatively independent of supply variation. When excessive positive supply voltages are encountered, zener diode D1 conducts, raising the potential at Q2's source and reducing Q1's base drive. Q1 comes out of saturation and limits the voltage applied to the chip. Reverse protection is provided by Q1's high emitter-base breakdown voltage.

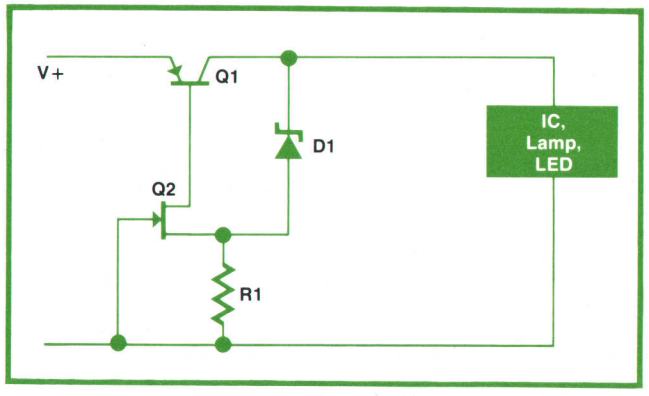
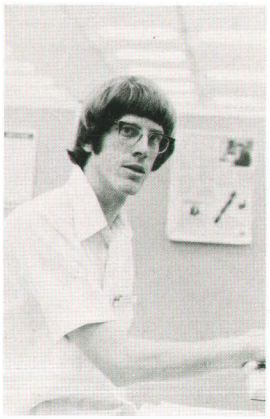



**Fig. 3.** *Power supply protection circuit protects the 545A's single integrated circuit, its tip lamp, and its latch LED against overvoltage and reverse voltage to ±25V.*

## SPECIFICATIONS
### HP Model 545A Logic Probe

**INPUT CURRENT:** ≤15 μA (source or sink)
**INPUT CAPACITANCE:** ≤15 pF
**LOGIC THRESHOLDS:**
TTL:
LOGIC ONE 2.0 + 0.4, −0.2 Vdc
LOGIC ZERO 0.8 + 0.2, −0.4 Vdc
CMOS: 3-10 Vdc supply
LOGIC ONE: 0.7 × $V_{supply}$ ±0.5 Vdc
LOGIC ZERO: 0.3 × $V_{supply}$ ±0.5 Vdc
CMOS: ≥10-18 Vdc supply
LOGIC ONE: 0.7 × $V_{supply}$ ±1.0 Vdc
LOGIC ZERO: 0.3 × $V_{supply}$ ±1.0 Vdc
**INPUT MINIMUM PULSE WIDTH:** 10 ns with ground lead (typically 20 ns without ground lead)
**INPUT MAXIMUM PULSE REPETITION FREQUENCY:** TTL, 80 MHz; CMOS, 40 MHz
**INPUT OVERLOAD PROTECTION:** ±120V continuous (dc to 1 kHz); ±250V for 15 seconds (dc to 1 kHz)
**PULSE MEMORY:** Indicates first entry into valid logic level: also indicates return to initial valid level from bad level for pulse ≥1 μs wide.
**POWER REQUIREMENTS:**
TTL: 4.5 to 15 Vdc
CMOS: 3 to 18 Vdc
MAXIMUM CURRENT: 70 mA
OVERLOAD PROTECTION: ±25 Vdc for one min.
**TEMPERATURE:** 0° to 55°C
**ACCESSORY INCLUDED:** Ground cable and grabbers (allows connection to IC pins).
**PRICE IN U.S.A.:** $125.
**MANUFACTURING DIVISION:** SANTA CLARA DIVISION
5301 Stevens Creek Boulevard
Santa Clara, California 95050 U.S.A.



**Robert C. Quenelle**

Bob Quenelle designed the 545A Logic Probe and put it into production. He's been with HP since 1973, and is now working on a software development project. Bob was born in Tucson, Arizona. He graduated from the University of Arizona at Tucson with a BSEE degree in 1970, and in 1973 he received his MSEE degree from Stanford University. He's married, lives in Santa Clara, California, and devotes part of his spare time to working with a local Boy Scout electronics Explorer post. He also likes camping and bicycling, and working in his garden or on electronics projects.

# A Multifunction, Multifamily Logic Pulser

*This microprogrammed pulse generator in a probe can produce single pulses, pulse bursts, or pulse streams. Its output stage automatically adjusts for the type of logic being stimulated.*

**by Barry Bronson and Anthony Y. Chan**

LOGIC PULSERS ARE VALUABLE tools for troubleshooting digital equipment. Using a pulser to inject pulses into logic nodes without cutting traces or removing ICs and monitoring the circuit response with a logic probe or clip is an effective method of locating logic, connective, or component faults. The pulser produces high-energy, short-duration voltage pulses of a logic state opposite to that of the node under stimulation.

As a logic stimulus element, the new HP Model 546A Logic Pulser (Fig. 1) offers features never before available in a self-contained probe. Operating from a 3-to-18V logic supply, it is capable of overriding TTL, DTL, HTL, and CMOS logic nodes with narrow pulses of automatically controlled voltage, polarity, and width, and selectable rate and count.

The new pulser retains much of the simplicity of its predecessor: one power connection, single push-button control, completely self-contained electronics, a normally high-impedance output tip, and low power consumption. It expands the basic pulser concept by providing additional features that aid digital design and troubleshooting. These include 10-Hz and 100-Hz low-duty-cycle pulse streams that can be used for continuous clocking of circuits or as a current injector for a current tracer, a pulse-per-second mode for slow clocking circuits and following the action at human speeds, and recurring bursts of 10 and 100 pulses for presetting sequential circuits (e.g., counters, shift registers, sequencers) with a precise number of counts. An LED annunciator on the tip provides feedback to identify the output mode and allow pulse bursts to be detected and counted. By programming single pulses and bursts of 10 and 100 while observing the LED, a predetermined number of outputs can be generated. A "smart" output stage takes care of pulse shaping and overload protection for compatability with all popular positive logic families.

Serial encoding of the six function modes on a single push-slide switch (similar in operation to that of a flashlight) allows rapid eyes-off programming and the ability to lock the pulser in any mode for continuous hands-off operation. To program a mode, the


**Fig. 1.** *Model 546A Logic Pulser provides single pulses, pulse bursts, and pulse trains that automatically drive a digital circuit node to its opposite state.*

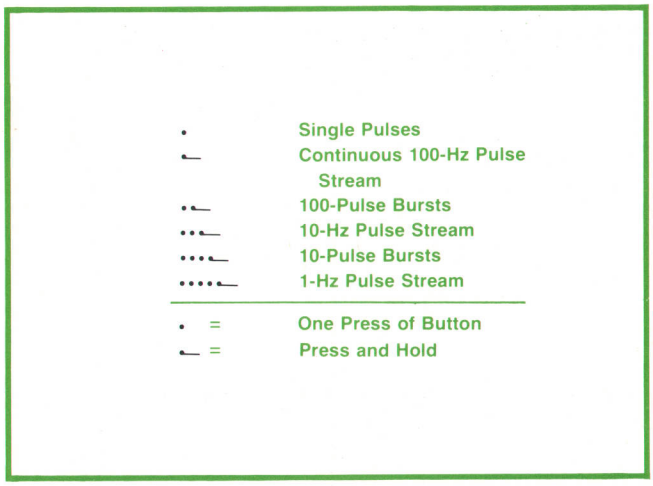



**Fig. 2.** *The logic pulser is programmed by means of a single button, using the code shown.*

button is pushed a predetermined number of times in rapid succession. Continuing to hold it down after the last push causes the selected function to be executed (see Fig. 2). Sliding the button forward forces it to stay down and locks the pulser in the mode selected. All switch debounce and sequence timing are implemented internally.

### Pulser Applications

The 546A Logic Pulser can serve as a stimulus instrument for locating many common digital IC problems. The response-measuring instrument can be a logic probe, a logic clip, or a current tracer. For example:

| Problem | Response Instrument |
|---|---|
| Shorted IC Input or Output | Probe, Tracer |
| Stuck Data Bus | Probe, Tracer |
| Internal Open in IC | Probe |
| Solder Bridge | Tracer |
| Sequential Logic Fault | Clip |
| Shorts to $V_{cc}$ or Ground | Probe, Tracer |

The pulser is a versatile design tool. It can be used to single-step breadboard designs, provide a substitute system clock, or verify the integrity of ground and power buses. In sequential circuits such as flip-flops, counters, and shift registers, the pulser can be used to preset, clear, or clock the circuit, or preload the circuit with a precise number of pulses.

The pulser has many applications in microprocessor and other bus-structured systems. For example, it can force the CPU into the reset mode, inject interrupts (single shot or 1, 10, or 100 per second), set flags and clear data latches in I/O ports, and force a memory write to occur at a selected address in RAM. The user can examine the data set up in a bus-driving IC by pulsing its bus-enable line and using a logic probe on its output bus, and check system data error detecting or correcting performance by injecting bit errors into a serial data transmission channel. When used with the 547A Current Tracer, the pulser can help locate faults on stuck buses.

### An Instrument on a Chip

Most of the electronics in the 546A Logic Pulser is on a single custom HP large-scale integrated circuit. The "instrument on a chip" concept keeps the parts count, size, power, and cost low. On-chip logic is a micropower version of low-power Schottky logic, and includes a 256-bit read-only memory (ROM), 14 flip-flops, and 41 gates. An on-chip voltage regulator contains a voltage and temperature compensated reference and control circuit for generating the 2.7V that runs the internal logic. The total operating current for the logic is less than 25 mA. Total power dissipation for all circuits on the chip is less than 100 mW.

Since most of the IC operates at low voltage, two sets of layout rules were adopted to minimize total chip area. Using high-density cells for low-voltage and lower-density cells for higher-voltage circuits, we were able to use our standard bipolar single-level metal process to put approximately 1000 transistors on a 2.7×3.2-mm die, and still have overvoltage protection to ±25V.

In Fig. 3 it can be seen that the 546A is a ROM-based system. The 256-bit ROM is a functionally optimized structure occupying less than 10% of the chip area. A free-running 100-Hz RC-controlled voltage and temperature compensated clock circuit, operating at 2.7V, acts as a time base for the instrument. Using an external resistor and capacitor allows better

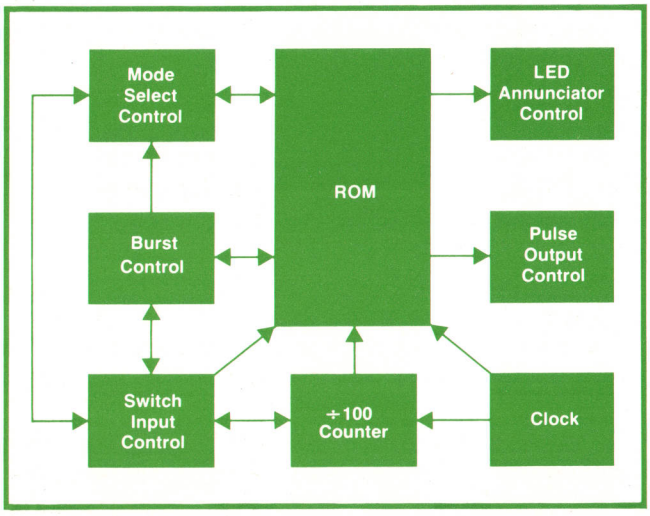



**Fig. 3.** *546A block diagram. Most circuits are on a single custom IC chip, including the 256-bit ROM.*

than ±10% accuracy over the full voltage and temperature range of the instrument.

The ÷100 counter acts as a scaler for generating pulse and LED output rates, a counter for the bursts, and a timer for program mode detection and switch debouncing. The switch input control debounces the single-contact switch, presets the ÷100 counter and burst control, generates a single-shot output signal, and increments the mode select control circuit. The mode select control determines whether the instrument is programming or executing a mode, which output mode it is in, and when to return to the standby mode.

The burst control governs the burst timing, count (98 or 6 for the first burst*, 100 or 10 for successive ones), and pause interval between burst outputs.

The LED annunciator circuit is a ROM-controlled direct-drive constant-current sink. It drives the high-efficiency LED in the tip.

### Automatic Output Control

An on-chip automatic pulse output control circuit effectively delivers the proper pulse polarity, voltage, width, and fast edge necessary to overdrive the logic node at the tip. It can output a 3V, 10-mA, 10-μs pulse to a 3V CMOS clock input node or a 5V, 0.5A, 0.5-μs pulse to a TTL line driver output. About 20% of the active chip area and 40% of the discrete components in the pulser are directly involved in this pulse output control task. Fig. 4 is a functional schematic of the output stage.

*98 and 6 burst counts are necessary to subtract out the 2 and 4 pulses that output when the user pushes the button to program the 100-pulse and 10-pulse burst modes.

Transistors Q0 and Q1 are normally off, and S0 and S1 are open. The pulser presents a high impedance to the logic node at the tip. Residual charge on coupling capacitor C1 has been bled off by R1.

When a signal from the ROM initiates an output cycle, the one-shot is triggered, and Q0 turns on via I0 (a 100-mA on-chip current source), G0, and the control 0 line. Immediately after Q0 saturates, S0 is closed through delay element D0, an on-chip capacitor/SCR circuit, and the 0 sense comparator is enabled. The load on the pulser tip is pulled toward ground through C1, a low-impedance ceramic capacitor. Current through C1 gets reflected as a voltage (dv= Idt/C1) on the sense line via input resistor R2 and speed-up capacitor C2. When the tip load current is low, as in CMOS, C1 charges slowly. Before it can reach 0.7V about ten microseconds elapses and the one-shot shuts off the 0 output circuit through G0. If a heavy load is present at the tip (e.g., a TTL buffer) charge develops rapidly on C1. When the voltage across C1 reaches 0.7V, the 0 sense comparator fires the overload line causing the one-shot to retrigger and the 0 output circuit to turn off. The heavier the load, the shorter

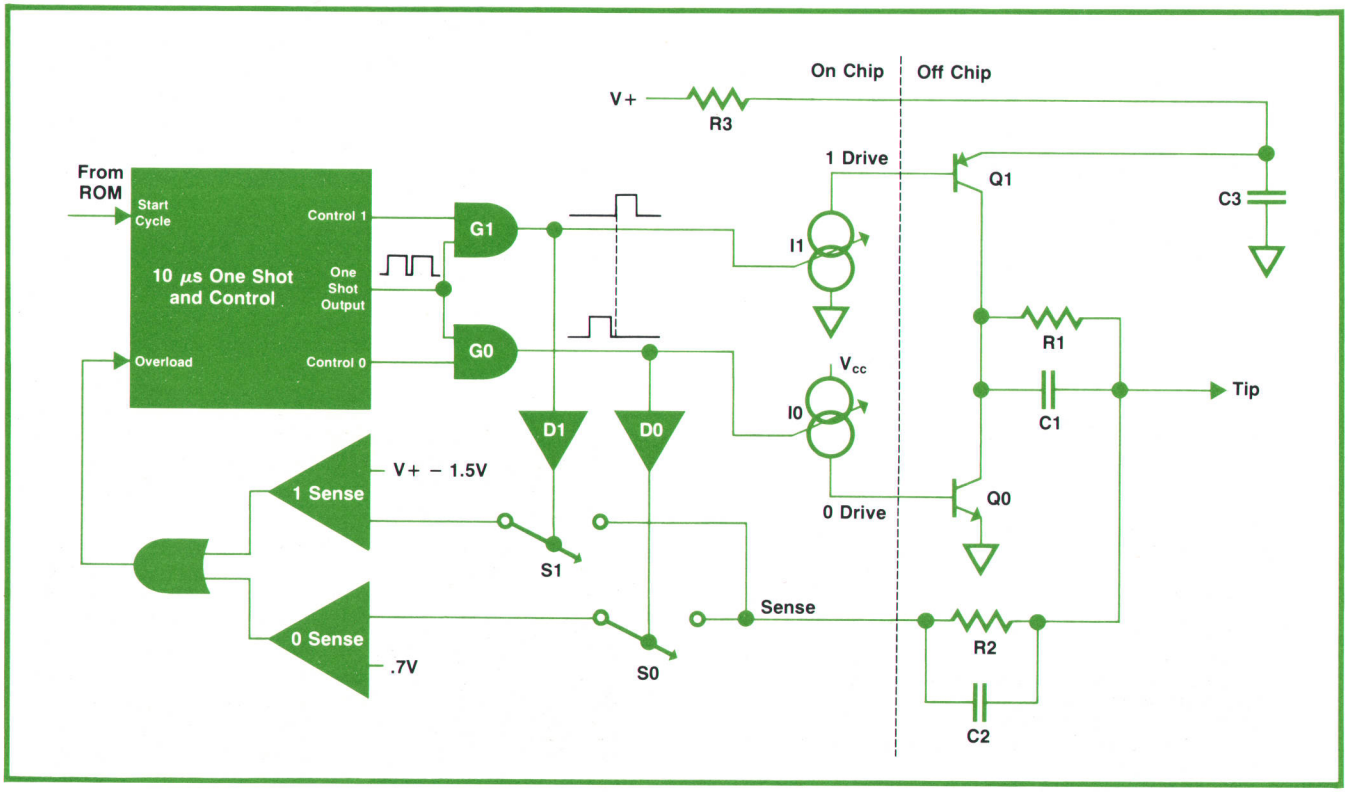



**Fig. 4.** *Functional schematic of 546A output stage. The circuit automatically delivers pulses of the proper polarity, voltage, width, and transition time to override the logic node at the pulser's tip.*

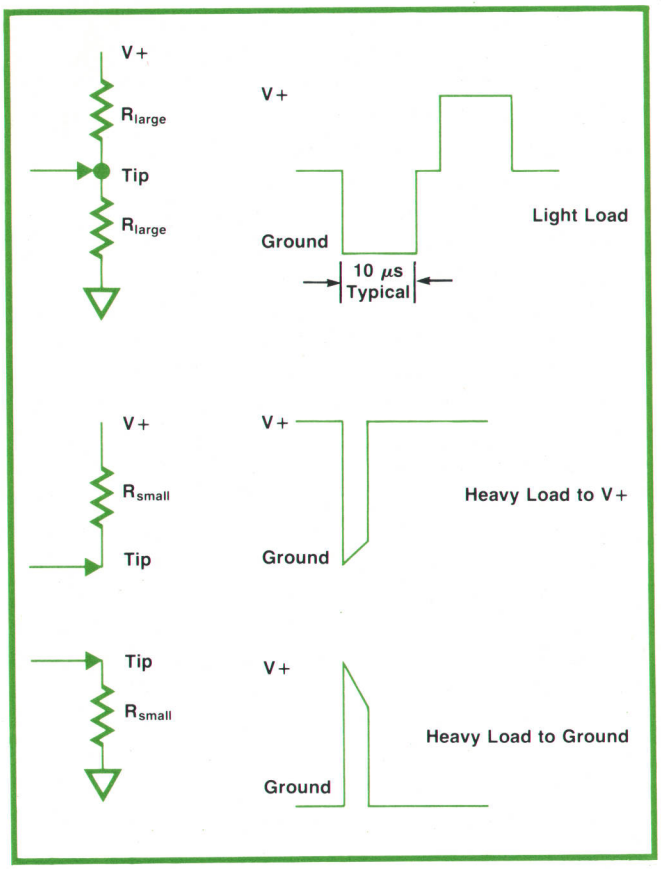



**Fig. 5.** *Typical 546A output waveforms under various loads.*

will be the output pulse. Active turn-on and turn-off of Q0 assure fast pulse edges through logic transition regions.

At the conclusion of a 0 output pulse, the 1 output circuit becomes active. Its operation is analogous to that of the 0 output circuit except for the variable threshold setting of the 1 sense circuit, necessary to adjust to the 3-to-18V operating range, and the inclusion of charge storage capacitor C3 and charging resistor R3. C3 sets the 1 output voltage pulse amplitude and decouples potentially large current surges from the tested circuit's supply line. Between output cycles, current through R3 restores the charge lost from C3 during the previous 1 output. R3 and C3 also provide good power supply ripple tracking. This assures accurate instantaneous pulse amplitude control when used with a poorly regulated CMOS power supply.

The pulse output cycle is complete when Q1 turns off. Fig. 5 illustrates output waveforms under various loads.

## SPECIFICATIONS
### HP Model 546A Logic Pulser

**OUTPUT:**

| Logic Family | Power Supply Voltage | Output Current |
|---|---|---|
| TTL | 4.5-5.5 Vdc | ≤650 mA |
| CMOS | 3-15 Vdc | ≤100 mA |

| Logic Family | Pulse Width | Typical Output Voltage High | Low |
|---|---|---|---|
| TTL | ≥0.5 μs | ≥3 Vdc | ≤0.8 Vdc |
| CMOS | ≥5 μs | ≥($V_{supply}$ −1 Vdc) | ≤0.5 Vdc |

TIP IMPEDANCE: <2 ohms active; >1 megohm off
SHORT CIRCUIT TIP PROTECTION: Continuous
IMPEDANCE: <2 ohms active; >1 megohm off

**POWER SUPPLY REQUIREMENTS:**
OPERATING VOLTAGE RANGE:
TTL: 4.5-5.5 Vdc
CMOS: 3-18 Vdc
Operating current; ≤35 mA
POWER SUPPLY INPUT PROTECTION: ±25V for 1 min.

**TIME BASE ACCURACY:** ±10%
**OPERATING TEMPERATURE:** 0° to 55°C
**ACCESSORY INCLUDED:** Ground cable and grabbers.
**PRICE IN U.S.A.:** $150.
**MANUFACTURING DIVISION:** SANTA CLARA DIVISION
5301 Stevens Creek Boulevard
Santa Clara, CA 95050 U.S.A.


**Anthony Y. Chan**

Tony Chan designed the custom IC chip for the 546A Logic Pulser. He joined HP in 1973 with four years' experience in linear and digital IC design. Before taking on the pulser.IC design, he developed low-power low-voltage logic gates. Tony was born in Hong Kong. He received his BSEE degree from the University of California at Berkeley in 1969 and his MSEE degree from California State University at San Jose in 1974. He's married, has two children and has a home in Sunnyvale, California that he's currently remodeling. He also enjoys working with wood and with automobiles.

**Barry Bronson**

Barry Bronson, project leader for the 546A Logic Pulser, received his BS degree in engineering from UCLA in 1970 and his MSEE degree from Stanford University in 1975. With HP since 1971, he's developed several automatic production test systems and contributed to the 5035T Logic Lab and the 5000A Logic Analyzer. Barry is a native of Los Angeles, California and now lives in San Jose. He and his wife have a one-year-old daughter. At home, Barry likes to work on electronics projects of his own, one of them a home-made microcomputer system. He also has a part-time video equipment business, dabbles in photography and the stock market, and plays tennis.

# Probe Family Packaging

**by David E. Gordon**

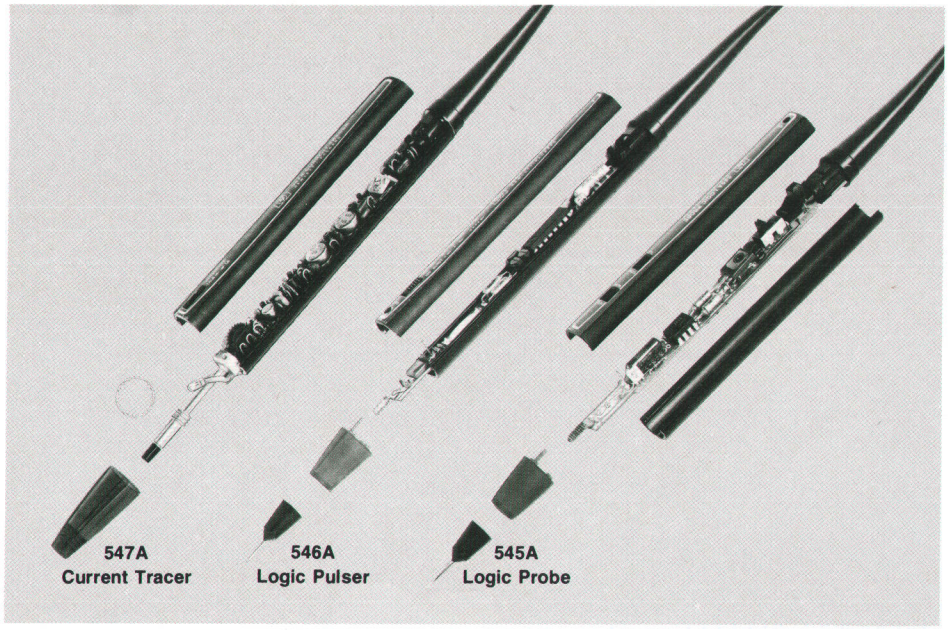



**Fig. 1.** *Probe housing design makes it possible to produce three instruments with a minimum number of different parts.*

The problem was to design a second generation probe packaging system for three new logic test instruments, accommodating 100% more circuit area with minimal instrument size increase, 200% more heat dissipation, and electromagnetic shielding. The amount to be spent for tooling was strictly limited. It was desirable that all parts be inexpensive, easy to assemble and service, and highly reliable.

Our solution was to use an aluminum extrusion coupled with simple molded plastic parts that snap, slide, and press together to provide a low cost, versatile instrument package that meets the functional requirements of the electronic design (see Fig. 1).

To have low factory and selling costs and stay within the tooling budget, the package had to be designed using a minimum number of parts that could be produced by easy manufacturing methods—aluminum extrusion, plastic molding, and metal stamping processes offered the necessary tooling to accomplish this. Ordering, stocking, and handling costs are reduced by using common parts, and the increased production volume of those parts lowers the manufacturing costs. For low assembly and service costs, all of the mechanical parts, with the exception of the crimp-on cable strain relief, are easy to fit together by hand without the use of nuts, bolts, washers, etc. (see Figs. 2 and 3).

Custom switches for the logic probe and logic pulser are produced at very low cost. The lighted pulse memory reset switch (Fig. 4) and the latching pulser mode switch use plastic actua-

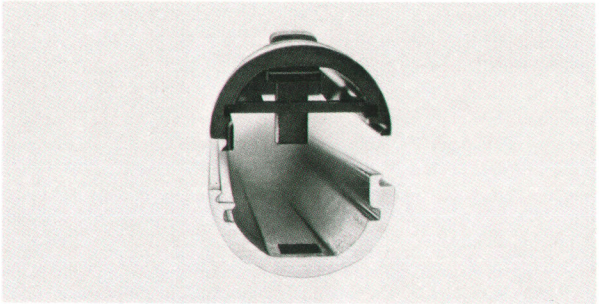


**Fig. 2.** *At top is an end view of the upper interlocking extrusion for the 546A Logic Pulser with the pulser switch in place. Internal slots serve as guides for the sliding switch. Slots in the lower extrusion serve as printed circuit board guides. Lower extrusion is from the 547A Current Tracer, showing the faced and clear alodined end that provides grounding of the case for electromagnetic shielding.*

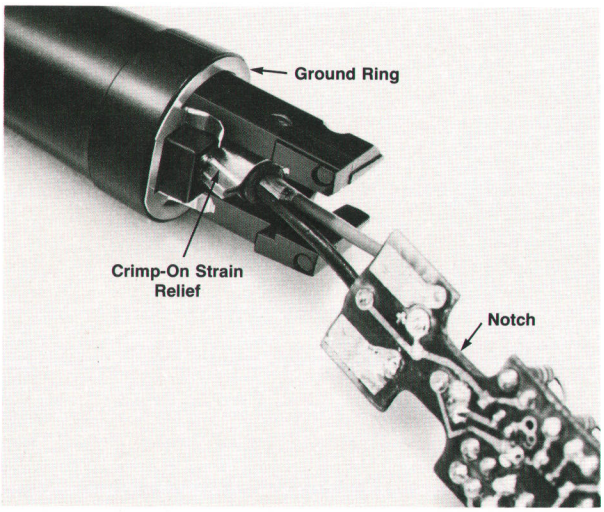



**Fig. 3.** *Ground ring provides a ground path from the bottom of the printed circuit board to the end of the extrusion shown in Fig. 2. Crimp-on strain relief pulls back into a cavity and locks the cable into place. Notches in the printed circuit board snap into the rear plastic support for structural ridigity.*

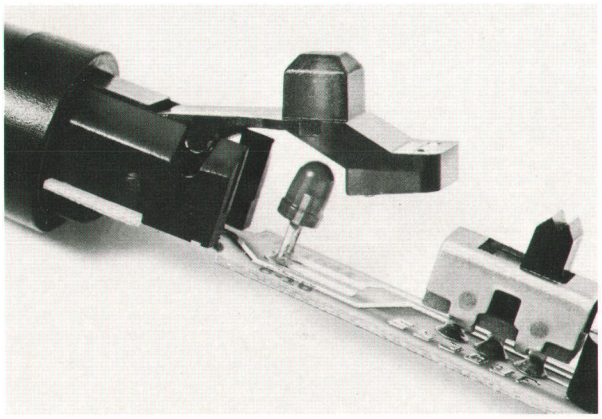


**Fig. 4.** *545A Logic Probe pulse memory switch rotates into place over LED. Press-in switch contact touches printed circuit traces when the button is pushed.*

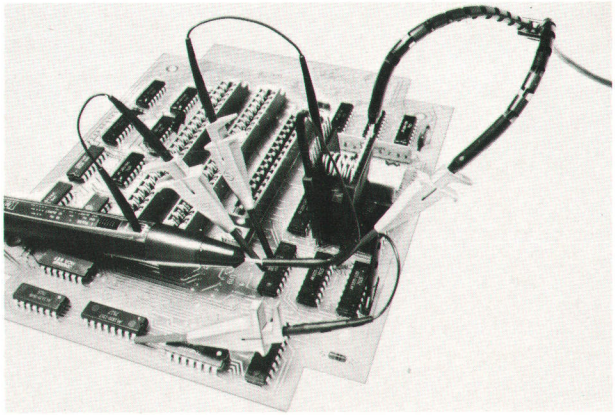


**Fig. 5.** *Probe interconnect system provides for connection of power leads, probe tip, and ground pin to standard test pins, an IC test clip, or HP grabbers.*

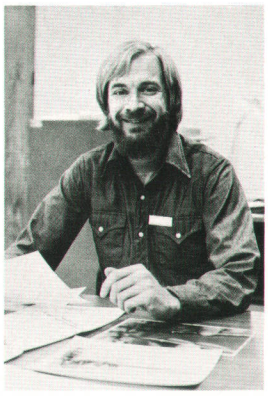
tors with printed circuit contacts to simplify manufacture and assembly.

The instruments use an interconnect system that provides for connection of the power lead, probe/pulser tip, and ground pin to either a standard test pin, an IC test clip, or an HP grabber (see Fig. 5).

Aluminum extrusion allows for a very versatile package, since it can be cut to any length. With minor secondary operations, five different body halves are produced. Perhaps the aluminum extrusion's greatest attribute is its excellent heat transfer, which keeps component temperature to a minimum for higher instrument reliability. Also, it provides electromagnetic shielding when grounded to the printed circuit board, making the sensitivity of the current tracer possible. The case surface is hard black anodized for the scratch resistance necessary for a high breakdown voltage, and the thin cross sectional area of the extrusion yields a larger circuit volume per unit length than previous plastic packaging.

**Acknowledgments**

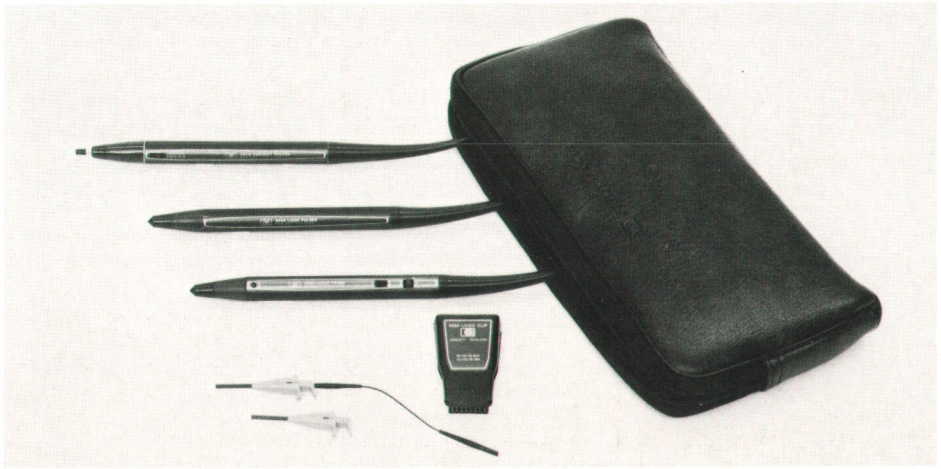
I would like to share design credit with Jim Marrocco, whose ideas and efforts contributed a great deal to the project. Also, considerable manufacturing assistance came from Steve Balog and John Lindahl.



**David E. Gordon**

Dave Gordon received his BSME degree from California State Polytechnic College at Pomona in 1973, and joined HP a month later. Now group leader for printed circuit multilayer process engineering, he served until recently as product designer for logic troubleshooting instruments. Dave was born in Alhambra, California, and now lives in Los Gatos, California, with his partner and her two children. Family activities and the "invigorating disciplines of meditation and Hatha yoga" are major interests; he also enjoys backpacking and cycling.

## IC Troubleshooting Kits



IC Troubleshooting instruments are available in kits consisting of various combinations of logic probe, logic pulser, logic clip, current tracer, logic comparator, and carrying case. Model 5022A Kit (shown) contains the four instruments described in this issue: the 545A Logic Probe, the 546A Logic Pulser, the 547A Current Tracer, and the 548A Logic Clip.

# Multifamily Logic Clip Shows All Pin States Simultaneously

*This new logic clip works with virtually all logic families from ECL to 18V CMOS. Loading of the circuit under test is minimal. The clip is protected against overloads to 30V.*

**by Durward Priebe**

A LOGIC CLIP IS A HANDY means of monitoring logic conditions in a digital integrated circuit (IC) system. It simultaneously clips onto all the leads of a dual in-line IC package (DIP) and displays the logic states of all pins of the device at once, instead of one pin at a time like a logic probe. Corresponding to each IC pin is one light-emitting diode (LED) on top of the clip; it turns on when the logic level on that pin is more positive than a specified threshold voltage. The user sees the logic states of all IC pins by observing the LED array, and can quickly identify state changes or verify truth tables. The clip is useful for system designers, test technicians, and field service personnel.

The new Model 548A Logic Clip (Fig. 1) was designed to provide this capability with a maximum of ease and versatility for the user while imposing negligible loading upon the IC being examined. Today's digital systems typically contain a variety of device types, along with microprocessors, memory, interfaces, and other functional blocks in NMOS, CMOS, TTL, ECL, and other logic families. The 548A was designed to be readily compatible with these types of devices. In most applications its operation is automatic; simply clip it onto the IC in any convenient orientation and observe the pin states shown by the LEDs. Power leads for the clip are unnecessary, since each clip pin has a network that seeks the most positive and negative voltage levels on the IC; from these the 548A draws its power and sets proper threshold levels. Each remaining clip pin is then free to compare the IC pin voltage with the internally derived threshold and control the illumination of the corresponding LED. Each IC pin sees a negligible nominal load of 3$\mu$A and 20 pF thus assuring that the clip does not perturb the IC's operation. Operation is automatic for positive supply voltages of 4 to 18 volts. Internal regulation maintains essentially constant LED brightness over this voltage range.

Many digital systems contain higher-voltage analog or interface DIPs, so it is possible that a user may inadvertently place the clip on such a circuit. The 548A is protected against this, and will not be damaged by momentary connection to an IC with a total voltage differential of up to 30V.

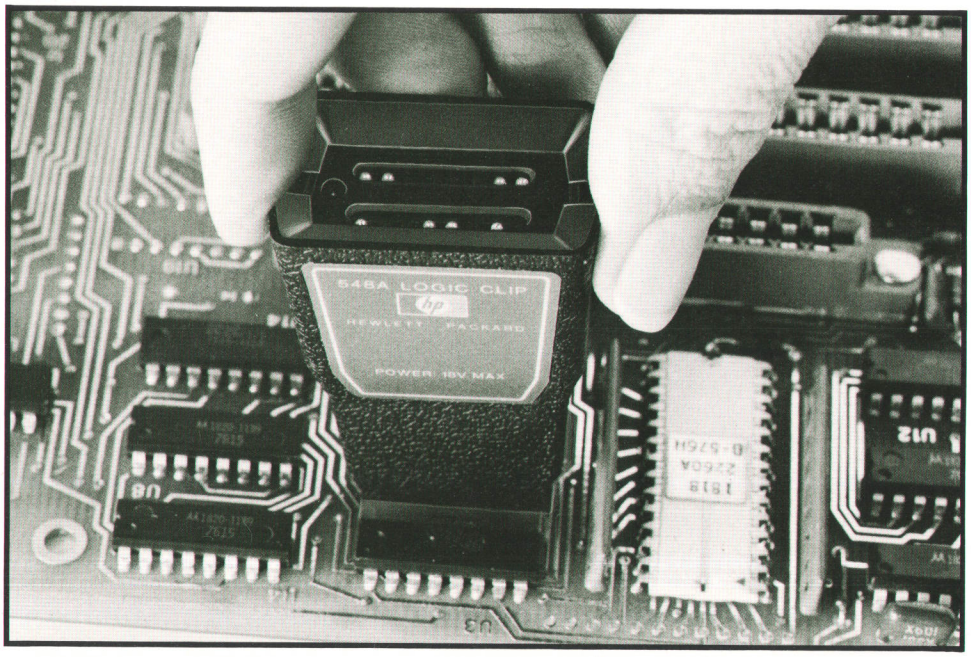



**Fig. 1.** *Model 548A Logic Clip simultaneously displays the states of all pins of ICs in dual in-line packages.*

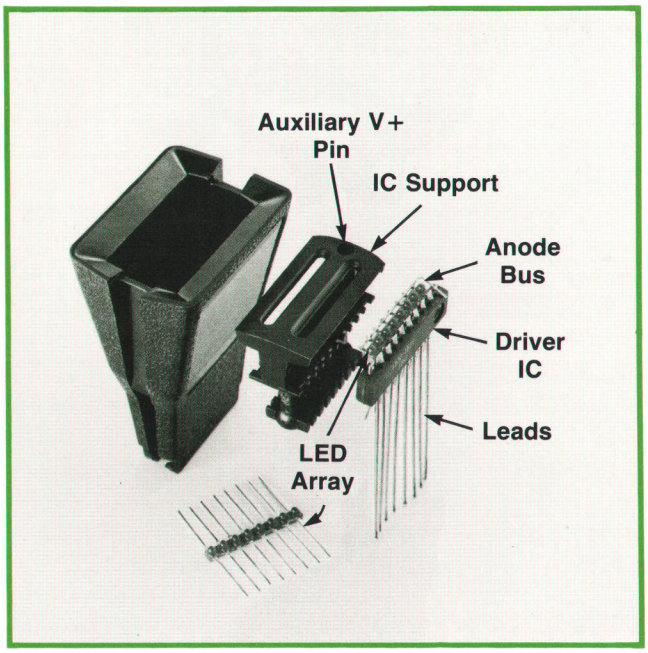



**Fig. 2.** *Internally, each half of the 548A Logic Clip consists of a 20-pin custom IC connected to a custom LED array.*

Threshold voltage is set nominally at 40% of the total IC supply voltage. This provides ideal levels for all of today's common logic families as shown in Table I.

**Table I**

*548A Logic Family Compatability*

| Logic Family | Supply Voltage | IC Worst-Case Output Logic Levels | Guaranteed 548A Input Threshold Range |
|---|---|---|---|
| CMOS | 4-18V | <.5V, >($V_{DD}$−.5V) | .34 to .46 × $V_{DD}$ |
| | 3V | <.5V, >2.5V | 1.5V nominal* |
| DTL/TTL | 5V | <.5V, >2.4V | 1.7 to 2.3V |
| HTL/HNIL | 12V | <2.5V, >7V | 4.1 to 5.5V |
| | 15V | <2.5V, >9.5V | 5.1 to 6.9V |
| NMOS | 5V | <.4V, >2.4V | 1.7 to 2.3V |
| ECL | −5.2V | −.9V, −1.7V typ | −1.4V nominal** |

*with +4.5V applied to 548A Auxiliary V+ connector
**with +5V applied to 548A Auxiliary V+ connector

### Auxiliary Connector Adds Versatility

An auxiliary V+ connector on top of the clip further extends its versatility. Although the worst-case clip current consumption is only 50 mA, this may be intolerably high, such as when troubleshooting a 3V battery-operated CMOS system. In such a system the IC supply voltage is also too low for normal 548A operation. However by connecting a +4.5V supply to the auxiliary V+ connector, 3V CMOS is readily tested; nominal threshold is 1.5V and no power is drawn from the IC supply.

This connector also aids examination of ECL ICs, since it provides a means of shifting the threshold voltage. Nominal threshold when using this connector is $0.4(V^+-0.8V)-0.6|V^-|$ which results in a threshold of −1.4V when the IC's negative supply is −5.2V and +5V is applied to the connector. The voltage on this connector must be maintained at least 1.5V higher than the IC's most positive pin but less than 20V higher than the most negative pin.

### Inside the Clip

The 548A is an integrated "silicon instrument." Internally each clip half consists solely of a 20-pin custom IC with an LED array attached, as shown in Fig. 2. The high-efficiency LEDs in the special HP array operate at only 1.5 mA nominal current. Together with low-power IC design, this results in the clip's typically requiring only 30 mA with 15 LEDs on at 5V, or just 10 mW of power for each comparator-driver-LED channel.

A simplified schematic of each channel is shown in Fig. 3. Each input pin is connected to two diodes and one input of a comparator. If an input is connected to the ground pin of the IC under test all the clip current flows to ground through the forward-biased D2 of that pin. Voltage on the $V_{cc}$ pin forward-biases its D1 and supplies power to the clip. All other pins then have both D1 and D2 reverse-biased. Special HP power Schottky diodes (on the chip) are used for D1 and D2, since high reverse breakdown voltage, low forward voltage, low reverse leakage current, and low capacitance are essential. Integrated Schottky diodes are also free of the parasitic elements associated with PN diodes that would destroy the very high imped-

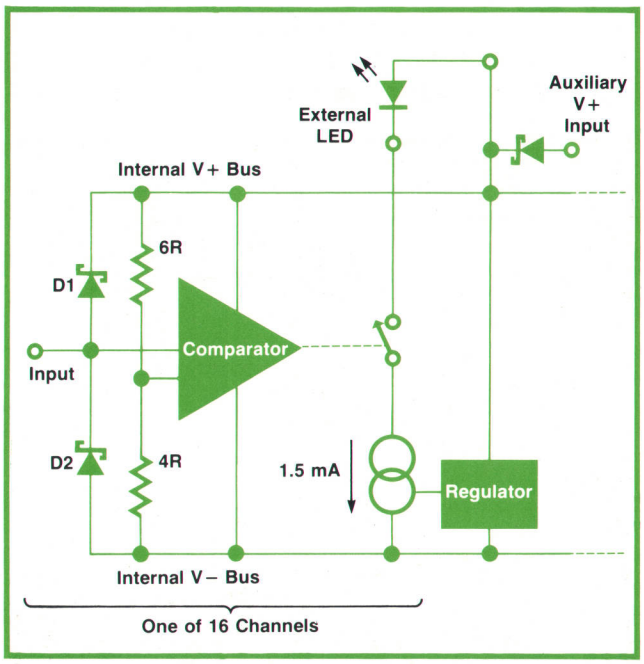



**Fig. 3.** *Simplified schematic of one 548A channel. Each channel detects whether it is connected to a ground pin, a power supply pin, or a logic pin of the IC under test and operates appropriately for that type of pin.*

ance of each input pin. The comparator input bias current plus the leakage currents of D1 and D2 sum to a typical 3μA input current; 15μA is the guaranteed maximum. The reference input of the comparator is connected to a resistor divider across the internal supply buses, while a regulator maintains constant LED current over the broad operating supply voltage range.

### Using the Clip

The clip can be used on standard DIPs with 8, 14, or 16 pins. To accommodate packages with more pins it's usually a simple matter to wire the signal lines of interest to a 16-pin dummy IC package added to the breadboard or printed circuit card. To make it useful on printed circuit boards with a high density of ICs or in cramped locations, the clip is physically small; it is 3.8 cm long and extends only 5.1 cm above the IC being examined. The LEDs are arranged in two rows of 8 with 0.1 in (2.54 mm) spacing between LEDs, and 0.3 in (7.62 mm) between rows. The LEDs are intentionally unnumbered to eliminate the confusion of the three sets of pin numbers that would be necessary for 8, 14, and 16-pin devices. Reliable electrical contact to the IC is assured through the use of gold-plated beryllium-copper contacts.

For convenience the clip may be oriented on the IC with the auxiliary V+ connector at the pin 1 end. This serves as a reminder of the location of the reference pin since the top of the IC is hidden from view by the clip.

To verify an IC's truth table the system clock must be made slow enough to allow recognition of each state. This is readily accomplished by disabling the clock and advancing it with the single pulse, 1-Hz, or 10-Hz modes of the 546A Logic Pulser. At clock rates above 20 Hz the clip provides some duty cycle information and indicates dynamic pin activity by LED brightness changes.

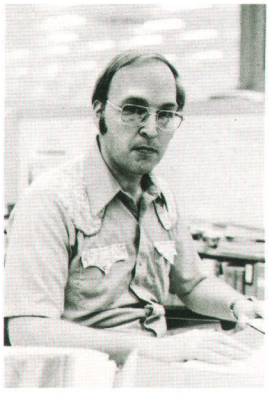

## Acknowledgments

The job of designing "silicon instruments" requires the marathon effort of many people. We would like to thank the IC layout staff for their help in designing the world's most complex jigsaw puzzles and the IC department for their help in building them (including testing and "finding missing pieces"!). These two groups helped accomplish difficult design goals and made these instruments possible. HP's Optoelectronics Division provided the innovative LED array for the logic clip. We would also like to thank Roger Smith, group leader, and Gary Gordon, section Manager, for their contributions and guidance. Pete LeMmon was instrumental in the development of the automatic test system. Lou deGive helped develop the manufacturing technology for the 547A current sensing tip. Roy Criswell and Mike Yarbrough coordinated development activities with the rest of HP, and Bruce Hanson was our marketing consultant.

*-John Beckwith*
*-Barry Bronson*
*-Anthony Chan*
*-Durward Priebe*
*-Robert Quenelle*


## SPECIFICATIONS
### HP Model 548A Logic Clip

**INPUT CURRENT:** ≤±15μA per pin
**INPUT THRESHOLD:** ≥(.40 ± .06) × supply voltage = logic high (e.g. at 5V supply, LED is guaranteed to be off below 1.7V and on above 2.3V)
**INPUT PROTECTION:** 30 Vdc for one minute
**INPUT VOLTAGE RANGE:** 0-18 Vdc
**POWER SUPPLY REQUIREMENTS:**
VOLTAGE: 4-18 Vdc across any two pins
CURRENT: ≤50 mA with 15 LEDs on
AUXILIARY SUPPLY VOLTAGE: 4.5 to 20 Vdc applied to connector. Supply must be ≥1.5 Vdc more positive than any pin of IC under test.
**TEMPERATURE:** 0°C to 55°C
**ACCESSORY INCLUDED:** Auxiliary power cable and grabber.
**PRICE IN U.S.A.:** $105
**MANUFACTURING DIVISION:** SANTA CLARA DIVISION
5301 Stevens Creek Boulevard
Santa Clara, California 95050 U.S.A.

**Durward Priebe**

Durward Priebe has been designing integrated circuits for 11 years. With HP since 1973, he's served as an IC consultant, most recently on the 545A, 546A, and 547A probe designs, and designed the 548A Logic Clip. He's authored several articles on ICs in technical publications. Durward was born in Melrose Park, Illinois and attended California Polytechnic College at San Luis Obispo, graduating in 1965 with a BS degree in electronic engineering. He and his wife have two children, live in Sunnyvale, California, and take great pride in doing most things themselves. Their concern for their city occasionally results in Durward's representing his neighborhood at city council meetings. Among Durward's other interests are taping local concerts, astronomy, ornamental welding, sailing, and photography.


### Corrections

A typographical error occurred in the equation given as an example of the printout modes for the HP-91 Calculator in last month's issue of the Hewlett-Packard Journal, page 10. The equation, for the length (L) of a belt connecting two pulleys, should be:

$$L = \pi d_2 + (d_2 - d_1)(\tan \psi - \psi)$$

It should also be noted that the equation is valid only for $d_2 > d_1$.

Part of one of the references given with the article on the HP Model 47201A Oximeter in the October issue was inadvertently omitted. Reference number 9 should be:
H. Poppius and A.A. Viljanen, "Non-Invasive Measurement of Oxygen Saturation during Exercise in Patients with Pulmonary Disease," XXVII Nordiske Lungelege Kongress, Oslo, Norway, 13-15 June 1976.

The first equation given on page 5 of the same article should be: $I = I_0 10^{-Kcd}$

# Interfacing a Parallel-Mode Logic State Analyzer to Serial Data

*A new serial-to-parallel converter enables a parallel-mode logic state analyzer to work with serial data so the analyzer's tabular display and versatile triggering can be used for tracing data flow in serial data systems.*

**by Justin S. Morrill, Jr.**

SINCE THEIR INTRODUCTION three years ago, logic state analyzers have become well established as indispensable tools for troubleshooting digital systems. By capturing a sequence of digital words appearing on a data bus or other multinodal location, and displaying the sequence as a table of binary words, logic-state analyzers enable the user to trace data flow and thus track down problems in his system.

These instruments were designed to work with parallel information (all bits of each word appearing simultaneously on parallel lines). Much digital activity, however, occurs serially (bits occurring sequentially on a single line). For example, many calculators operate serially, and data is transmitted over phone lines in serial form. Furthermore, many parallel-

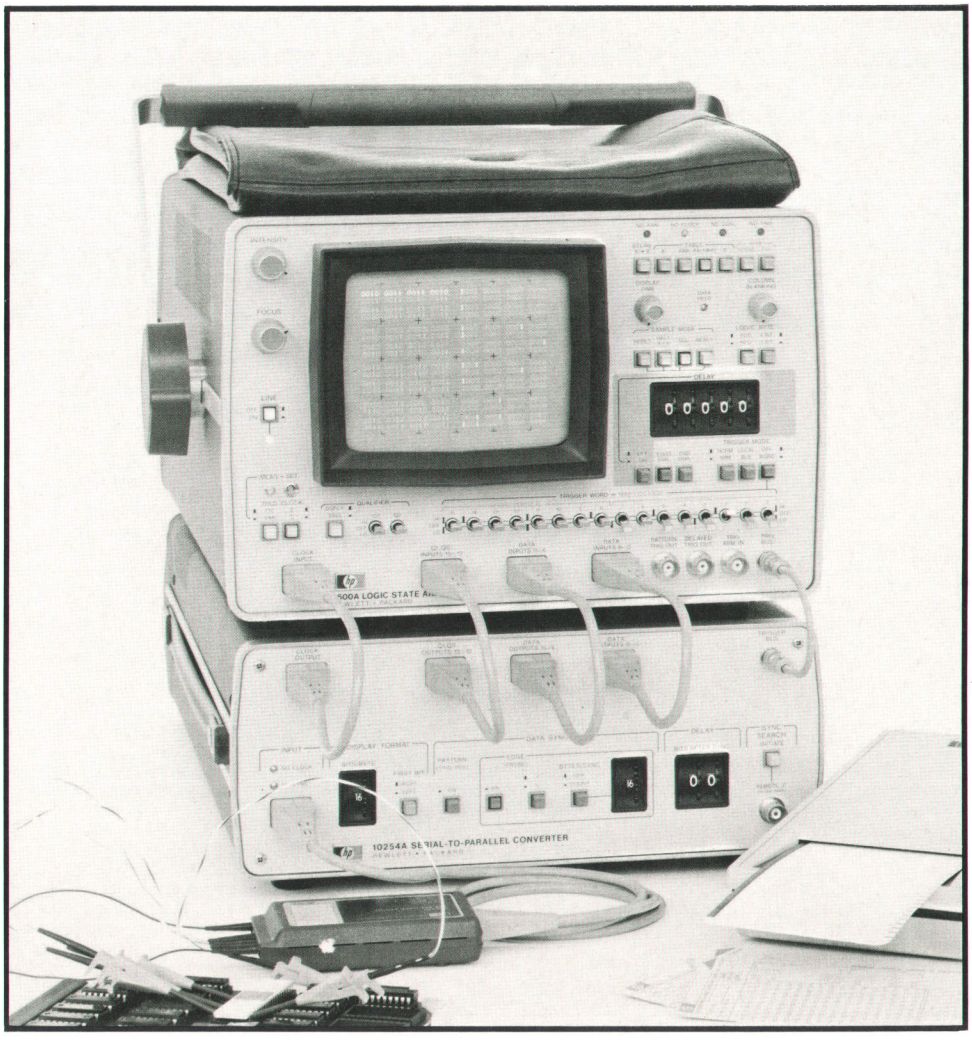


**Fig. 1.** *Model 10254A Serial-to-Parallel Converter (lower unit) interfaces Model 1600A Logic State Analyzer (upper unit) to serial data streams so serial data flow occurring at a node or on a bus can be presented as a table of binary words on the logic analyzer's display. The usefulness of this instrument combination for production test is enhanced by the Model 10253A Card Reader (lower right) that enables data sequences marked on cards to be stored in the logic state analyzer; bit-by-bit differences between the stored sequence and actual data flow then appear as brightened 1's on the right half of the display.*

mode digital systems perform some operations serially, such as at I/O interfaces for disc memories and teletypewriter consoles.

A new serial-to-parallel converter now makes it possible to use the measurement capabilities of HP's Model 1600A and 1607A Logic State Analyzers for the serial data domain. This accessory, Model 10254A, accepts data in serial form and formats it into a parallel word for presentation as one line on the logic state analyzer's tabular display (Fig. 1). Just as with parallel data, the logic state analyzer can be set to capture and display the data sequence beginning with a particular word, or data leading up to the word, or data at some point downstream from the word, enabling the user to search out and find the part of the program where malfunctions occur.

Applicable too are all the other operating modes of the 1600A/1607A Logic State Analyzers (halt when the captured sequence differs from a previously stored sequence; indicate bit-by-bit differences between captured and stored sequences, etc.).[1] When the 1600A and 1607A are both used at the same time with the 10254A Serial-to-Parallel Converter, both serial and parallel data, such as that occurring on both sides of an I/O interface, can be displayed side by side in two tables on the 1600A display.

### What It Does

The heart of the Model 10254A Serial-to-Parallel Converter is a bidirectional shift register that is loaded with the serial data. The parallel outputs of the register are applied to the inputs of the logic state analyzer, and when a clock counter indicates that a full byte has been loaded into the shift register, a clock pulse is sent to the logic state analyzer. The clock pulse causes the byte to be stored in the analyzer's memory where it becomes available for display as one line on the analyzer's CRT.

Designed-in flexibility enables the converter to be used for a wide variety of applications. For example, the shift register is bidirectional so serial data can be loaded in either direction. This gives the user a choice of having the first bit appear in the most significant position (LEFT) on the analyzer's display, or in the least significant position (RIGHT), whichever is easier for him to interpret.

The length of each byte can be selected to be anywhere from 1 to 16 bits by the BITS/BYTE selector switch. Words longer than 16 bits are handled as two or more sequential bytes.

The data stream bit that is to be loaded into the shift register as the first bit can be determined in a number of ways. Frequently, a sync or framing pulse is available somewhere in the machine being tested. This pulse can be used to initiate loading of the data stream. If, however, the desired data occurs some time after the sync pulse—say following a preamble and address—the BITS AFTER SYNC selector can be used to delay data loading for a predetermined number of bits (up to 99) after the sync pulse.

If, on the other hand, no separate sync pulse is available, the SYNC SEARCH mode can be used in conjunction with the pattern recognition capabilities of the logic state analyzer. In this mode, the serial system clock pulses are sent to the logic state analyzer continuously, causing it to read the contents of the

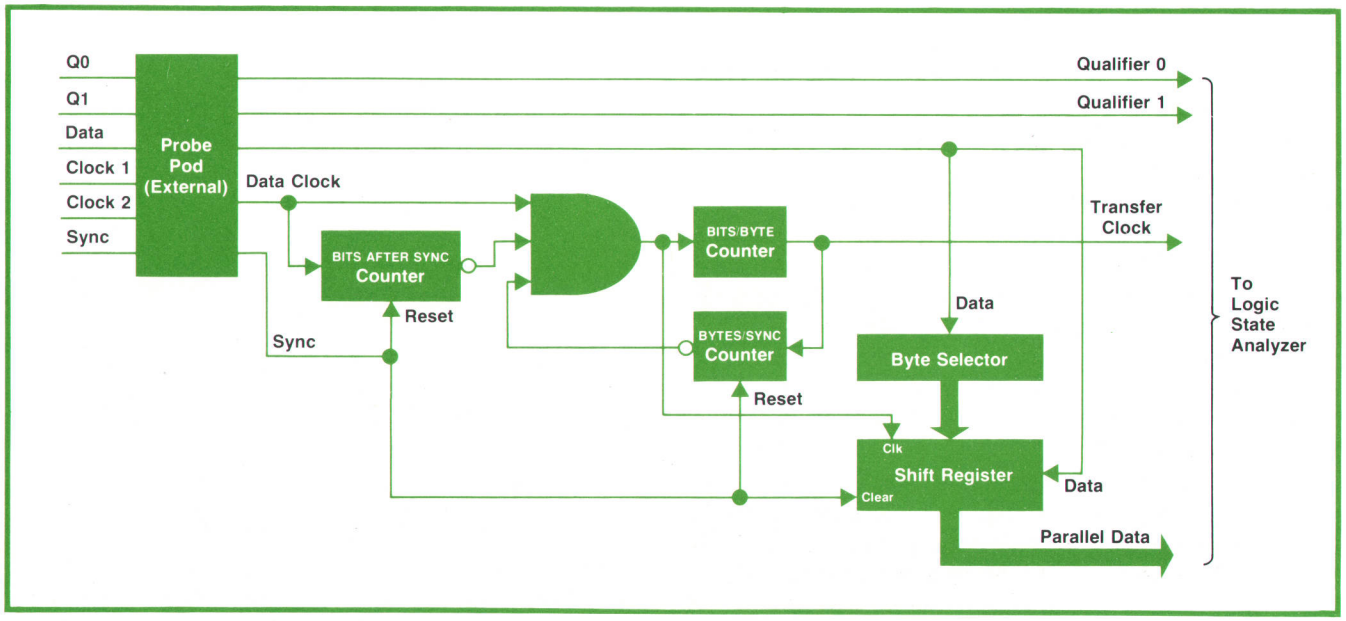



**Fig. 2.** *Simplified block diagram of Model 10254A Serial-to-Parallel Converter. Serial-to-parallel conversion occurs in the shift register. The other blocks control the timing and direction of shift register loading and the timing of data transfer to the logic state analyzer.*

10254A shift register each time a new bit is entered. When the register contents match the digital word set up on the analyzer's TRIGGER WORD switches, the resulting trigger is sent to the serial-to-parallel converter, causing it to revert to normal operation. Clock pulses are then sent to the logic state analyzer only when a complete new byte is entered, as determined by the setting of the BITS/BYTE switch. Initiation of normal byte transfer, however, can be delayed past the trigger event by any number of bits up to 99 by use of the BITS AFTER SYNC delay selector.

By use of the DELAY selector switch in the logic state analyzer, the data displayed can be moved downstream from the trigger event. The DELAY selector determines the number of bytes (up to 99,999) that must occur after the trigger event before display of the data sequence starts. It is thus possible to go far into a serial word and precisely locate and capture data for display.

### Selective Store

The data transferred to the logic state analyzer can also be qualified by the BYTES/SYNC selector to compress the amount of data stored for display. This switch selects the number of bytes transferred following each sync pulse. For example, if only the two 16-bit bytes that occur 27 bits after sync are of interest, the BYTES/SYNC selector is set to 2, the BITS/BYTE selector is set to 16, and the BITS AFTER SYNC is set to 27. Then only those two bytes, out of possibly many serial words, would be captured for display.

Further qualification of the data stored for examination can be obtained by use of the two qualifier selector switches on the logic state analyzer. Two qualifier inputs are provided on the serial-to-parallel converter's input probe and these inputs are latched through the converter to the analyzer. Bytes will not be stored in the analyzer unless these inputs match the settings of the switches (1, 0, or DON'T CARE), enabling further selectivity in the data captured for storage.

### Technical Details

A block diagram of the serial-to-parallel converter is shown in Fig. 2. Inputs are by way of the same type of six-probe pod used with the Models 1600A and 1607A Logic State Analyzers. Besides the data input, there is a sync input, two qualifier inputs, and two clock inputs (OR'd internally into a single clock input). The pod has level-sensing circuits that decide whether the voltage sensed by each probe is a 1 or a 0. The threshold level, variable over a range of ±10 V, is set by the controls on the logic state analyzer.

An operating feature that was considered of paramount importance was that the data supplied to the logic state analyzer should always be justified to the right. This is because the logic state analyzer column-blanking control, which allows the user to blank out unused columns when bytes are less than 16 bits, starts on the leftmost column and blanks columns successively towards the right. This causes no problem when the first bit in a serial data stream is to be in the leftmost column. Data is entered at the right-hand input of the shift register and stepped to the left with each clock pulse until the complete byte is in the register and the byte is transferred to the logic state analyzer.

When the first bit is to be in the rightmost column, however, the data must be entered at a point in the shift register corresponding to the length of the byte, then stepped to the right. With reference to the diagram of Fig. 3, an example will show how this works. Suppose each byte is to have 7 bits. The BITS/BYTE switch then sets up the selector gates such that the

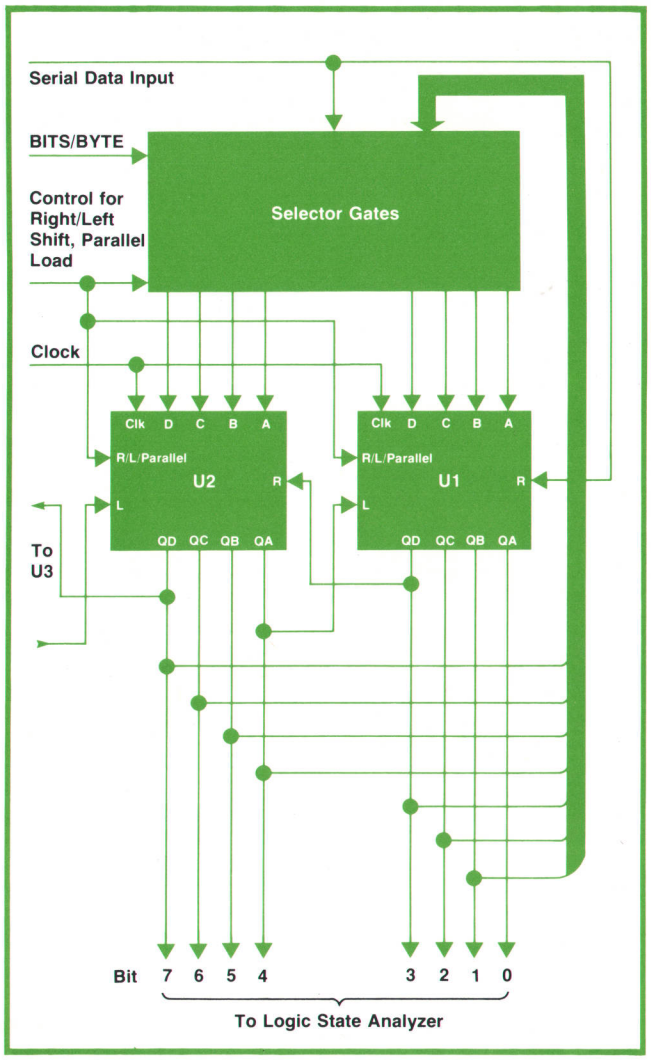



**Fig. 3.** *Block diagram of part of the bidirectional shift register. U1 and U2 are commercial IC 4-bit shift registers (U3 is the next IC in the 16-bit shift register chain). The selector gates enable serial data to be loaded through any bit position during right-shift operation (see text).*

data stream is routed to the parallel input of the shift register that is 7 units from the right-hand end, in this case input C of U2. At the same time, U2's parallel output QC is routed back through the selector gates to parallel input B, and QB is routed to A.

Each clock pulse loads U2 in parallel, hence the bit in each stage of U2 is loaded into the adjacent stage to the right. The last stage output, QA, goes to the left input L of U1 where it is stepped to the right in the normal right-shift fashion. Thus, after seven clock pulses, the first bit loaded into C of U2 is in stage A of U1, the bit 0 position. The byte is thus right justified when it is transferred to the logic state analyzer.

## SPECIFICATIONS
### HP Model 10254A Serial-to-Parallel Converter

Requires an HP Model 1600A or 1607A Logic-State Analyzer to form complete measurement unit; uses data probe supplied with logic state analyzer as input device.

**DISPLAY FORMAT**
- BITS/BYTE: 1 to 16 (displayed as one line on logic-state analyzer)
- FIRST BIT (LEFT/RIGHT): formats displayed data with most significant bit left or right.

**DATA SYNC**
- PATTERN: synchronizes on digital pattern within serial data stream; pattern is selected by logic state analyzer's TRIGGER WORD switches.
- SYNC SEARCH: pushbutton or positive-going pulse (5V max) initiates search for pattern sync.
- EDGE: synchronizes on input probe sync signal with positive or negative edge selectable.
- DELAY (BITS AFTER SYNC): selects number of clock pulses (0 to 99) between sync signal and start of data acquisition.
- BYTES/SYNC: acquires 1 to 16 bytes between sync pulses for display.

**PROBE**
- REPETITION RATE: ≤10 MHz in EDGE sync; ≤7 MHz in PATTERN sync.
- INPUT RC: 40 kΩ shunted by ≤14 pF at probe tip.
- INPUT THRESHOLD: ±10 V dc selected at logic state analyzer.
- MINIMUM PULSE WIDTH: 40 ns at threshold.
- SETUP TIME: 50 ns (minimum time data must be present prior to clock transition).
- HOLD TIME: 0 ns (minimum time data must be present following clock transition).
- SYNC OCCURRENCE: 60 ns (minimum time sync edge must precede clock transition corresponding to first data bit).

**GENERAL**
- POWER: supplied by 1600A or 1607A logic state analyzer through interconnecting data cable.
- SIZE: 284mm W × 121mm H × 414mm D (11-3/16 × 4¾ × 5/16 inches).
- WEIGHT: 3.2 kg (7 lb )

**PRICE IN U.S.A.:** 10254A, $975. Note: data probe not supplied; uses data probe from 1600A or 1607A Logic State Analyzer.

**MANUFACTURING DIVISION:** COLORADO SPRINGS DIVISION
1900 Garden of the Gods Road,
Colorado Springs, Colorado 80907 U.S.A.


### Acknowledgments

Initial product definition was by Jeff Smith and many ideas were contributed by section manager Bill Farnbach. Product design was by Roger Molnar.


### Reference


1. C.T. Small and J.S. Morrill, Jr., "The Logic State Analyzer, a Viewing Port for the Data Domain," Hewlett-Packard Journal, August 1975.


**Justin S. Morrill, Jr.**

A native of Houston, Texas, Justin Morrill attended Rice University there, earning a Bachelor of Arts degree in Science and Engineering and a Master of Electrical Engineering. He then joined Hewlett-Packard (1972), initially working on an investigative project involving storage CRTs, then on the 1600A/1607A Logic State Analyzers. Since then, he has been designing accessories for the 1600A/1607A (card reader, serial-to-parallel converter, probes). When available time coincides with good snow conditions, Justin enjoys cross-country skiing. Otherwise, he goes cross-country in his four-wheel-drive vehicle. He also does some hiking and backpacking. He and his wife have one son, 3.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