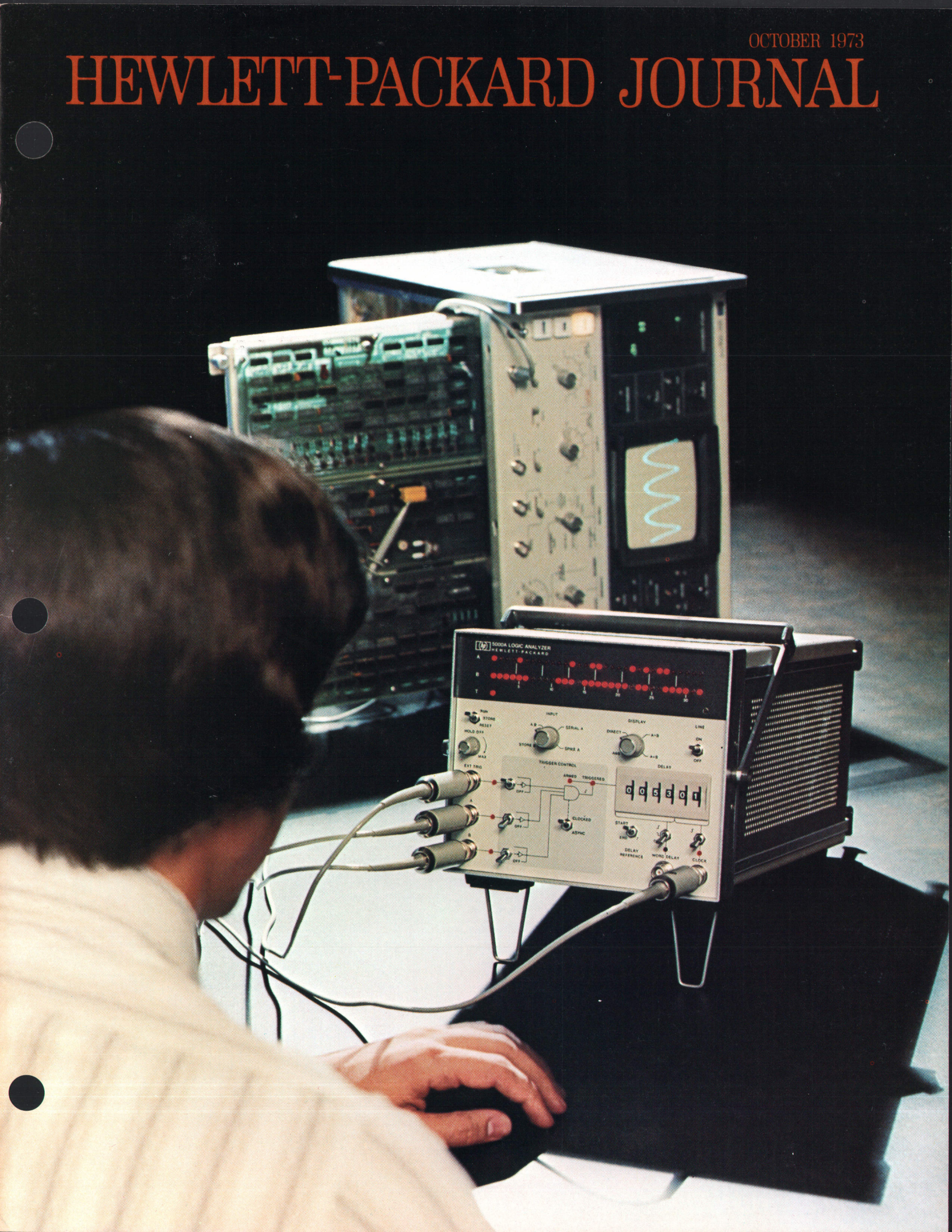
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The Logic Analyzer: A New Instrument for Observing Logic Signals

Designed specifically to solve digital design and troubleshooting problems, this new instrument provides a digital display with storage, positive and negative digital delay, combinatorial triggering, and digital sequence comparison.

by Robin Adler, Mark Baker, and Howard D. Marshall

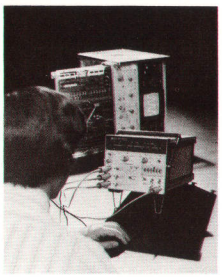
DIGITAL CIRCUITS confront designers and troubleshooters with measurement problems that differ in many ways from those in analog circuits. As a result, instruments developed for analog measurements are often less than optimum for the new digital measurements, so there is a need for new kinds of instruments designed specifically to solve digital problems.

Model 5000A Logic Analyzer, Fig. 1, is just that. An entirely digital instrument for displaying logic signals, it has a digital display, digital functions, and digital controls, and it operates in a manner that is intuitive to digitally oriented users.

A good example of the kind of problem that is easily solved by the Logic Analyzer is observation of long and infrequent logic sequences in calculators and other ROM-controlled systems. With conventional instruments, seeing these sequences is quite difficult and identifying individual bits is virtually impossible. With the Logic Analyzer and its digital storage, once-per-keystroke calculator sequences are easily captured. The Analyzer's digital delay makes it possible to observe any section of a thousand-bit sequence with no uncertainty as to which bits are displayed and no need to count clock pulses. These abilities also make it easy to see and analyze the long, non-repetitive signal sequences that occur in serial data transmission, such as between remote terminals and a computer.

Another problem arises in disc drives and other motor-driven computer peripherals. Continuous variations in drive-motor speed may cause so much jitter in the data waveforms that they are impossible to interpret when observed by conventional means. The Logic Analyzer's digital delay removes the jitter, so the display is stable and easily interpreted.

Other Logic Analyzer features are useful in a variety of digital applications. In its SPIKE mode, the Analyzer captures and stores the short, randomly occurring noise pulses that often cripple entire systems while escaping detection by conventional means. Negative delay helps the user analyze causes of errors in single-shot data sequences by displaying data that occurred prior to a trigger point. And a trigger point need not be defined simply as an edge occurring at a single node; the Analyzer can be set to trigger on coincidences of logic HIGH's or LOW's at two or three nodes.



Cover: *Model 5000A Logic Analyzer's two rows of 32 red light-emitting diodes display digital data occurring at the A and B inputs. A lighted LED indicates a logic HIGH level. Other LED's indicate the trigger point, input conditions, arming, and triggering. Designed specifically for digital design and troubleshooting, the Logic Analyzer simplifies many difficult measurements.*

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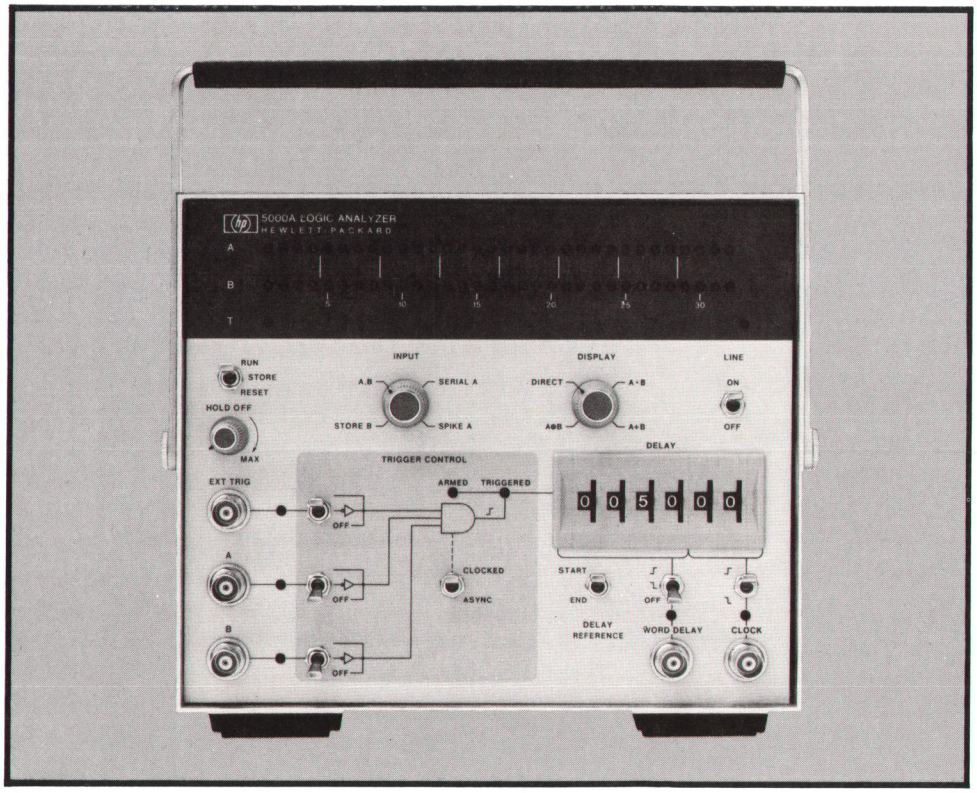


Fig. 1. *Model 5000A Logic Analyzer's two rows of 32 light-emitting diodes display the sequences of logic states at the A and B inputs. Positive and negative delay, combinatorial triggering, storage, spike detection, and several display modes help solve a multitude of digital measurement problems in design and troubleshooting.*

Clocked Light-Emitting-Diode Display

The Logic Analyzer displays 32 bits of digital data on each of its two rows of red light-emitting diodes (LED's). Each LED row displays data from one of the Analyzer's two data inputs, Channels A and B. The LED's turn on to indicate logic HIGH's and turn off for logic LOW's (Fig. 2).

The horizontal parameter of the display is time, proceeding from left to right. Time is quantized into discrete intervals according to the clock signal of the circuit or system under test. Thus the LED's represent the logic states of the data inputs during each of 32 successive clock cycles. The system clock signal is applied to the Analyzer's CLOCK input and serves to synchronize the Analyzer with the system under test.

How does this display compare to the more familiar oscilloscope display of logic waveforms? They are very similar, the Analyzer deleting some oscilloscope information and emphasizing other parameters more pertinent to digital needs. Oscilloscopes display voltage versus time; the Analyzer display quantizes each of these parameters, voltage into logic state and time into clock cycles.

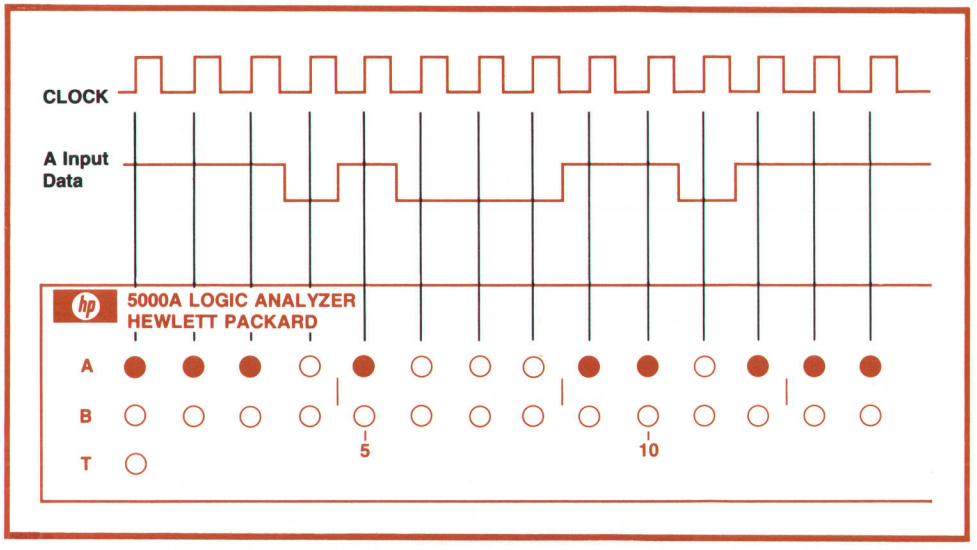


Fig. 2. *Logic Analyzer displays bits as defined by the clock signal of the system under test. A lighted LED indicates a high logic state. Either edge of the clock pulse may be selected as the data sampling point.*

Omitted from the Analyzer's display is analog voltage and timing information. These of course, are the signal parameters over which the digital designer has least control. Once he has selected a particular IC family, he cannot, for example, adjust high-state output levels or propagation delays beyond the limits specified on data sheets.

What the user does control is what the Analyzer is designed to display, that is, the procession of logic states as a function of clock cycle, or in other words, the function of the circuit. On and off LED's correspond naturally and intuitively to HIGH and LOW logic states. Using the test system's clock for the horizontal quantization means the data is displayed in terms of bits—just the information the user needs to compare circuit response to device truth tables or system timing diagrams.

Oscilloscopes, on the other hand, force the user to make the quantization into bits. To do this, he must display the clock along with the data and visually divide the continuous data stream into the bits of interest. At the same time the user must mentally impress the threshold voltage of the logic family on the waveforms to make decisions about HIGH's and LOW's.

This is not to say that either instrument precludes use of the other. Both are essential, although for different things. The oscilloscope is most important early in the design cycle, when questions about ringing, race conditions, fan-outs, and power distribution are important. These are questions that need to be answered before the system begins to run. Later in the design cycle, when the sequences of logic states are most important, and in production test and field service, the Logic Analyzer is likely to be more useful. There are also many measurements (often involving the Analyzer's digital delay) that can be made only by using both instruments together.

Digital Combinatorial Triggering

Triggering begins the Analyzer's data input and display processes. The trigger point is the reference point to which all following events are related.

The Analyzer's controls provide for triggering on either single events or multiple events occurring simultaneously. This capability is necessary in digital applications because digital systems commonly function in response to parallel data patterns occurring simultaneously on several circuit nodes. A device, for example, might be designed to accept data only when two control lines are HIGH concurrently. Therefore, synchronizing a measurement with the start of a process often requires the ability to recognize multiple simultaneous events. This the Analyzer can do. It triggers on an AND combination of up to three signals or their complements.

A major Logic Analyzer design consideration was that all controls be simple to use and intuitively understood by digital users. The trigger section is a good example. All trigger switches are grouped in a shaded area on the front panel (Fig. 3). The algorithm describing trigger requirements is drawn on the front panel as a simple schematic diagram using common digital symbols.

Triggering requires a high-going edge at the output of the front-panel AND gate. Trigger data can originate at three inputs, A, B, and EXT TRIG, reaching the AND gate via the slope-control toggle switches in each of the three paths. When any of these three-position switches is set to the upper position, data is transmitted directly from the associated data input to the AND gate. With the switch in the middle position opposite the inverter, data is inverted before application to the gate. In the lower or OFF position, the input is removed from the trigger process.

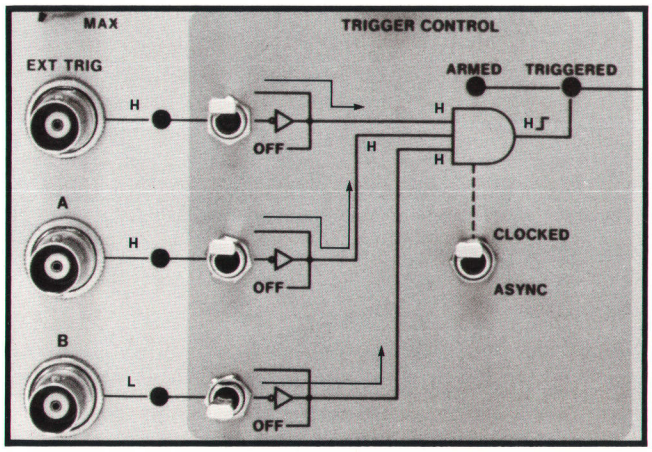


Fig. 3. *Trigger event that determines the start of the display is defined by a combination of up to three HIGH or LOW logic states and a positive or negative-going edge. Here the Analyzer is set to trigger when there are logic HIGH's at the A and EXT TRIG inputs and a logic LOW at the B input, and the selected clock-pulse edge occurs.*

With this arrangement the user can select any three-bit combination of HIGH's and LOW's as his trigger word. With the slope control switch up, the input must be HIGH for triggering; with it opposite the inverter the input must be LOW.

In ASYNC mode, when the AND gate pulses HIGH, the TRIGGERED light flashes immediately to indicate triggering. In CLOCKED mode, the AND output must remain HIGH until sampled by the clock.

Displayed data is always retained until new information is written over it after a subsequent trig-

Logic Analyzer Applications in Digital System Waveform Measurements

Wherever oscilloscopes are used to display digital information, the Logic Analyzer will be a valuable addition to the user's test equipment. Specific areas include computers, magnetic tape and disc drives, card readers, teleprinters, paper tape readers, point-of-sale readers and terminals, calculators, digital data transmission, ROM-controlled instruments, and others.

Disc Drives

Magnetic disc drives are fast-access, mass storage devices that record information on rotating magnetic platters or discs. Data is stored and read serially. The address of each data record on the disc is contained in a preamble that precedes the record and is part of the serial data stream. When the contents of a given record are desired, its address is entered and the data stream is monitored for that address. When the address is detected, a comparison circuit generates a pulse and data transmission begins. If this pulse is used to trigger an oscilloscope or Logic Analyzer, subsequent data is viewable. However, the preamble data has already passed by; seeing it requires a negative delay. The 5000A's END mode provides negative delay and makes it possible to see the address and other information stored in the preamble.

Looking farther into the data record following the trigger creates other difficulties. The timing of the waveforms depends on the rotational speed of the disc, which continually varies. Hence the waveforms jitter with respect to the trigger. Jitter is cumulative and becomes quite large several thousand bits into the record. Stable presentation of jittering data requires digital delay. A particular data bit always occurs a fixed number of clock cycles into the record, even though the time delay between the trigger and the bit of interest varies widely. Dialing this delay into the Logic Analyzer's thumbwheel register will produce a stable display of any desired bit.

The Logic Analyzer's single-shot storage simplifies finding and analyzing intermittent faults, which are common in disc drives and other computer systems. When a system fails once per hour or even less often, the 5000A will, whenever the error occurs, capture a sweep of data and hold it indefinitely. With negative delay, data that preceded the error can be displayed so the cause of the error can be analyzed.

Microprogrammed Devices

Microprogrammed, read-only-memory-controlled devices commonly generate long non-repetitive data sequences that are difficult to analyze. Calculators are a good example of such devices. A program to calculate the square root of a number might contain over ten thousand bits and repeat only as often as the square-root key is pressed.

In troubleshooting a ROM-controlled instrument, it may be possible to single-step through long sequences. However, this is often inconvenient, and the problem may go away at slow speeds. The Logic Analyzer allows the system to run at its normal rate while the test is being made. It can display not only data sequences but also spikes or transients on critical control lines. In cases where ROMs control arithmetic operations involving several shift registers, the Analyzer can be used to display in detail the complex operations that take place in these shift registers. This analysis capability goes far beyond merely observing the final result of a complex operation.

The Logic Analyzer's digital display, digital delay, and single-shot storage also simplify calculator measurements. The digital clocked display presents data and program instructions in the form of bits, just as they appear on timing diagrams or ROM truth tables. Storage captures the transient waveforms. If RZ (return-to-zero) encoding is used, SPIKE A mode will produce the desired display.

Because the serial instructions or data are usually grouped into words, digital delay by both bits and words is useful. With once-per-word pulses applied to the Analyzer's WORD DELAY input, any word can be displayed without counting pulses to find it. Bit delay within the selected word is helpful when word length exceeds the display capacity.

Digital Data Transmission

In digital data transmission, characters, words, and blocks of data take the form of fast single-shot bursts of ones and zeros. This is true whether the data is being transmitted between a terminal and a computer, between two data banks via modems and telephone lines, or between a frequency counter and a calculator in a small automatic test system. The Logic Analyzer easily displays these bursts. The Analyzer display is locked to the data by the clock and the Analyzer triggers only when data is received. Successive characters can be displayed one after another and stored as long as desired.

To access a specific part of a data block, such as a preamble, a postamble, a control bit, or a parity bit, the Analyzer's positive and negative digital delay can be used. If a trigger can only be found at the end of the preamble, engaging negative delay by selecting DELAY REFERENCE "END" will display the data that leads up to the trigger, namely the preamble. With exactly the same trigger point, the end of the data block can be observed by dialing in the correct amount of positive delay and retransmitting the data.

Analyzer and Oscilloscope

The synergism that exists between the Logic Analyzer and the oscilloscope is most evident when either instrument is used as a trigger source for the other. When the Analyzer's countdown of bit and word delays is complete, a pulse that can be used to trigger an oscilloscope is generated at the rear panel TRIG OUT connector. The 5000A's combinatorial triggering and digital delay combine with the oscilloscope's voltage and timing information to display analog parameters of hard-to-locate data bits. Stable oscilloscope displays of disc data or calculator program words are possible with this technique.

With a delayed-sweep oscilloscope, the reverse arrangement is often fruitful. Triggering the Analyzer from the delayed gate output of the oscilloscope begins the 5000A data input at the start of the intensified region on the oscilloscope CRT. The oscilloscope delay vernier can be used to scan rapidly through the waveform searching for suspect data. The Analyzer simultaneously displays the precise bit structure of the scanned data and indicates any spikes that are present. Searching for a particular control character in a serial transmission to or from a data terminal is a good example of the type of problem that can be solved using this technique.

(Continued on page 6)

(Continued from page 5)

Everyday Uses

While the examples given so far have concentrated on dramatic applications of the Logic Analyzer in difficult system measurements, the Analyzer will probably be used most often as a general-purpose bench instrument in common digital troubleshooting situations. For example:

- With the CLOCK input connected to the clock line of a flip-flop and the channel A input connected to the Q output of the flip-flop, the flip-flop can be checked for proper divide-by-two operation, indicated by a display of alternately off and on LED'S.
- An AND gate has pulses at its two inputs but the output remains LOW. Combinatorial triggering can determine if the inputs are ever HIGH simultaneously.
- With digital delay determining the number of clock pulses between overflows, proper division ratio in a programmable frequency divider is easily verified.
- The output pulse of a monostable multivibrator (one-shot) may be viewed using asynchronous triggering and SPIKE mode, no matter what the pulse relationship of the clock to the one-shot output.
- Data bits dropped in a recirculating shift register can be detected by comparing the circulating data with a stored reference.

ger. If only a single trigger occurs, the data is held indefinitely. The result is automatic, single-shot storage. There is no need to realize beforehand that data is non-recurring and engage special storage controls.

Even if a data sequence is repetitive, the Analyzer can be commanded to store it by placing a front-panel switch in the STORE position. With this same switch in the RUN position the display will change each time a trigger occurs. An adjustable HOLDOFF control prevents triggering for up to five seconds in the RUN mode so new data can be displayed at a convenient rate. At the end of the holdoff period an ARMED light on the front panel turns on to indicate that the Analyzer is ready to trigger.

Digital Delay

Normally, once the Analyzer has triggered, the next 32 bits of data at the A and B inputs are displayed. Other sections of the data sequence can be displayed using the positive and negative delay capabilities of the Analyzer. Positive delay, expressed as a number of clock pulses (or a number of word pulses and a number of clock pulses), is dialed into front-panel thumbwheels, and delay equal to the indicated number of pulses is inserted between triggering and the beginning of the display (Fig. 4). Thus the 32-bit "display window" is movable up to 999,999 bits (or 9999 words and 99 bits) downstream from the fixed trigger point, and there is no doubt as to which bits are being displayed.

Why *digital* delay? In synchronous systems, the clock signal is the prime mover; all signal sequencing is in response to it. Systems are designed so timing is in terms of numbers of clock pulses rather than their duration. An example is a system that might be set to generate an output pulse 1024 cycles after a start command. That this interval might happen to be 0.509 ms long is almost unimportant; the 1024 clock cycles are the significant point.

When the clock frequency is continually changing, as in a disc drive, this is even more significant. Here the time delay between the start of data transmission and a particular data bit is continually varying. The number of clock periods in the interval, however, is fixed, so digital delay will locate the desired data bit without jitter.

Digital delay is also useful when data streams are extremely long. Calculator sequences are an example. When trying to find a particular bit in a several-thousand-bit sequence, digital delay to the desired bit is the only way to get there and be certain of it.

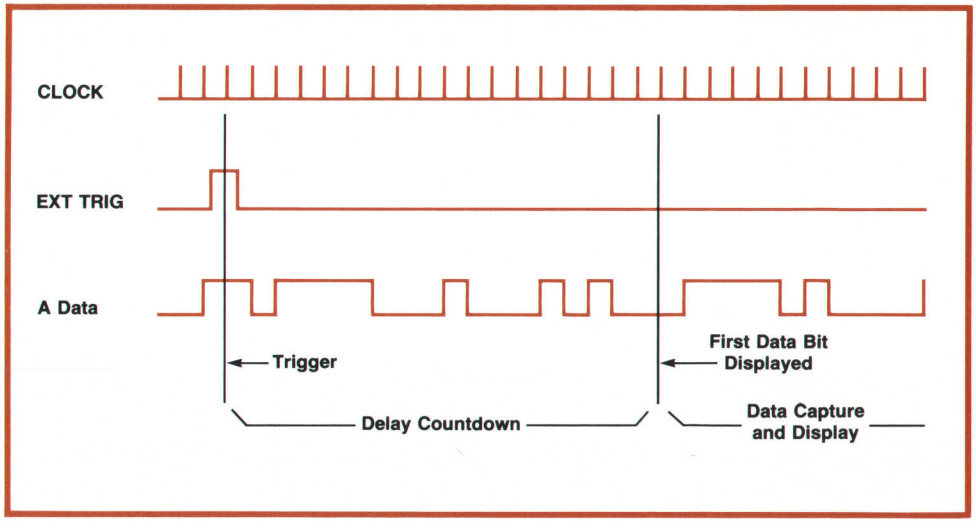


Fig. 4. *Preset digital delay is counted down between the trigger event and the start of the display. Here the Analyzer triggers when there is a logic HIGH at the EXT TRIG input, and display begins after an 18-clock-pulse delay.*

Negative Delay

Some oscilloscopes use an analog delay line to preserve information close to the trigger long enough for the CRT to display it. The 5000A extends this concept using digital storage to permit display of events up to 32 clock cycles before the trigger.

Negative delay is engaged by setting the DELAY REFERENCE switch to the END position. The trigger then occurs at the end of the display registers and the data displayed is the data that occurred on the 32 clock cycles prior to the trigger.

Uses of negative delay are numerous. For example, when analyzing serial trigger circuits in disc drives or data terminals, the serial word leading up to and causing the trigger can be displayed. Or, triggering from an error condition, the pre-error data may be examined to locate the cause of the error.

Input and Display Modes

In its most common mode of operation the Logic Analyzer is a two-channel device with a row of LED's for each channel. The various INPUT and DISPLAY modes use the two inputs and displays in other ways to perform additional functions. SERIAL A mode, for example, cascades the B display register onto the end of the A display. The result is a single 64-bit display loaded from the A input, and a single-channel 64-bit negative delay capability, as well. STORE B provides selective use of the Analyzer's storage. B-channel data is stored while the A display reloads with each trigger.

SPIKE A mode captures short, intra-clock-period pulses caused by noise or other problems (Fig. 5). These would ordinarily be missed by the Analyzer's normal once-per-clock-cycle sampling of the data inputs. High-going pulses occurring at the A input are displayed in the A register and low-going pulses in the B register. One reason SPIKE mode is necessary is that without it RZ (return-to-zero) data would either be undisplayable or undistinguishable from NRZ (non-return-to-zero) data.

The settings of the DISPLAY mode switch select various Boolean combinations of A and B input data for display. AND (A • B), OR (A + B), and EXCLUSIVE-OR (A ⊕ B) combinations are possible. Results appear in the A display; the B display is blanked.

A ⊕ B mode in conjunction with STORE B is especially useful in production test applications. EXCLUSIVE-OR is a comparison function; the result A ⊕ B is HIGH only when A and B are different. A ⊕ B mode allows rapid digital comparison of two supposedly identical data streams with any differences appearing as lighted LED's. Using

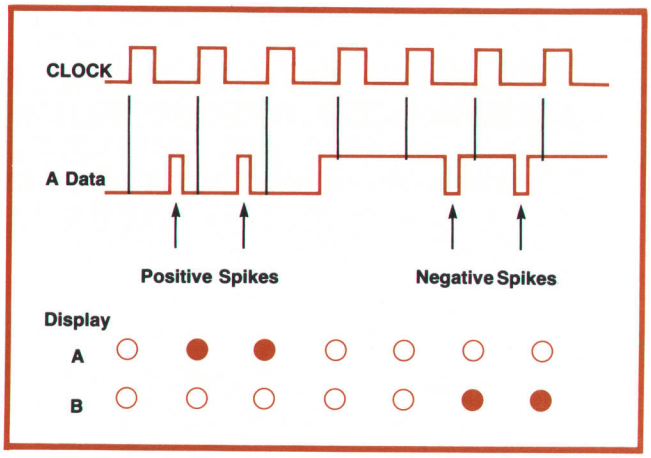


Fig. 5. *Spikes occurring between clock pulses may be desired signals or noise. In SPIKE A mode, the Analyzer displays spikes and shows whether they are positive-going or negative-going.*

STORE B mode, the B data may be loaded once and retained indefinitely, a useful capability when data from a reference device is being compared with data from one or more test devices (Fig. 6).

Getting Into the Analyzer

To minimize loading of circuits under test regardless of their IC family, each of the Logic Analyzer's five input channels (A, B, EXT TRIG, WORD DELAY, and CLOCK) has high input impedance: 1 MΩ in parallel with 25 pF. This also permits use of



Fig. 6. *A ⊕ B mode, one of three possible combined-waveform display modes, is useful for comparing test and reference circuit boards in production testing. Only differences are displayed.*

the Analyzer with standard Hewlett-Packard high-impedance probes and their accessories to further minimize circuit loading and to maximize probing flexibility.

The input channels are essentially identical. Each acts as a threshold detector to compare a high-impedance, low-level input to a dc threshold level and produce a logic signal indicating whether the input is HIGH or LOW. The inputs share a common threshold voltage, which is set by rear-panel controls. Two selectable threshold ranges are provided, each with its own voltage control. The high range covers ±1.4 volts and the lower one ±0.14 volts. The actual threshold voltage can be monitored at the rear panel for precise threshold adjustment. With 10:1 divider probes, effective thresholds are 10 times the values indicated on the rear panel. Thus ±14 volts of threshold variation is possible, sufficient to cover requirements of all types of digital integrated circuits.

Although the Analyzer is specified for clock repetition rates up to 10 MHz, the actual equivalent bandwidth of the signal inputs is greater than 50 MHz. This relatively high bandwidth is necessary to minimize skew between input channels and to provide high sensitivity to narrow input pulses.

The basic circuit of each input amplifier is illustrated in Fig. 7. Q1A and Q1B, a matched FET pair, are used in a totem-pole voltage-follower configuration to form a unity-gain amplifier. CR1 and CR2 clip excessive input signals to provide protection against overloads of ±200 V dc or ±400 V transient. U1 is a high-speed, high-gain analog comparator IC with complementary TTL outputs.

As an added convenience to the user, each input channel drives an LED annunciator that indicates the logic state of that input. Each annunciator functions as a logic probe, turning on to indicate logic

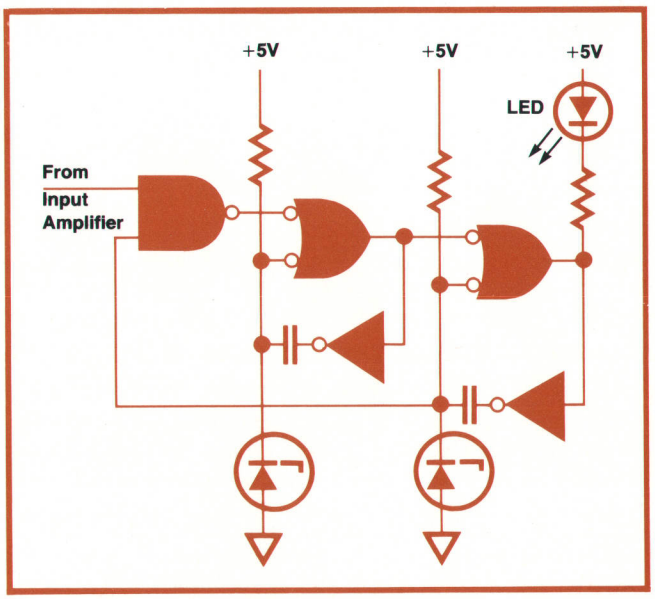


Fig. 8. *At each input is an LED annunciator that acts like a logic probe. LED turns on when the input is HIGH and off when it is LOW. Pulses are stretched to give a visible flash.*

HIGH's and off for logic LOW's, and flashing at a rate of a few Hz for pulse-train inputs. The annunciator circuit (Fig. 8) includes a pulse stretcher so the user can easily see the presence of single-shot or low-repetition-rate pulses, often very difficult to detect. The threshold voltage can be quickly set by connecting one of the inputs to a voltage equal to the desired threshold and adjusting the threshold control until the annunciator barely turns on or flickers.

Data Capture

The data on the A, B, and EXT TRIG channels goes from the comparator in the input amplifiers to the input flip-flops, where it is sampled and

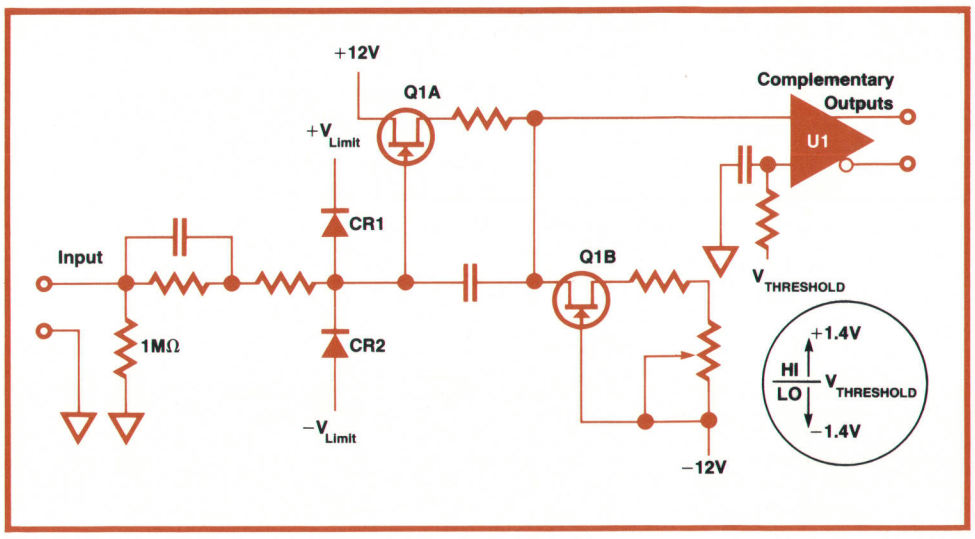


Fig. 7. *High-impedance input amplifiers minimize circuit loading. Variable threshold assures compatibility with all IC logic families.*

quantized into bits. Data at the inputs to these flip-flops is transferred to their outputs at the clock pulse edge selected by the slope control on the front panel. This takes place whenever there is a clock signal present. However, the display is not loaded until the Analyzer is triggered and all digital delay is counted to zero. When this occurs, data is transferred to the input registers a short time (50 ns) after it is loaded into the sampler flip-flops. (See block diagram, Fig. 9.)

For easier use and interpretation of the Analyzer and its display, the first bit in each display row represents the data at the A or B input when the trigger event occurs. It is also necessary that these first and subsequent bits be displayed immediately, as soon as they are sampled, without waiting (e.g., for the next clock pulse). To accomplish this the contents of the input samplers are continuously monitored for the trigger event. When it occurs, a delayed version of the input clock is gated to the input registers to load the contents of the samplers for display. On each succeeding clock pulse data is loaded into the samplers and 50 ns later is transferred to the input registers by the delayed clock. Loading continues in this way until the two 32-bit channels are filled.

Meanwhile, data has also been flowing from the input registers to the display registers. Details of this process are described in the section headed "Display Considerations."

Once loaded, data is frozen for a minimum of 50 ms before a new trigger and input sequence can begin. This guarantees that even an intermittent bit is displayed long enough to be recognized.

Triggering

One of the most difficult problems to overcome in the display of any waveform is the definition of a trigger or sync point to which the data can be referenced. It is necessary that the trigger, however defined, be a unique event, one that occurs only once in the cycle of the machine whose waveforms are being analyzed. When signals are repetitive, this guarantees that triggering always occurs at the same point in the sequence and, most importantly, that the display will be stable.

Examination of trigger requirements in synchronous systems reveals several possibilities. First, the trigger may be well defined as an event on a single line—for example, start-program pulses, reset pulses, or gating signals. In this case, the familiar single-channel, edge-sensitive triggering is sufficient and the positive or negative edge of the pulse provides a unique data reference. It is crucial that an edge rather than a level serve as the trigger since the pulse may extend over many clock periods. The edges are unique; the level is not.

If the trigger cannot be derived from a single line, several signals can be ANDed together to provide the unique reference. This is controlled using the Analyzer's three trigger control switches.

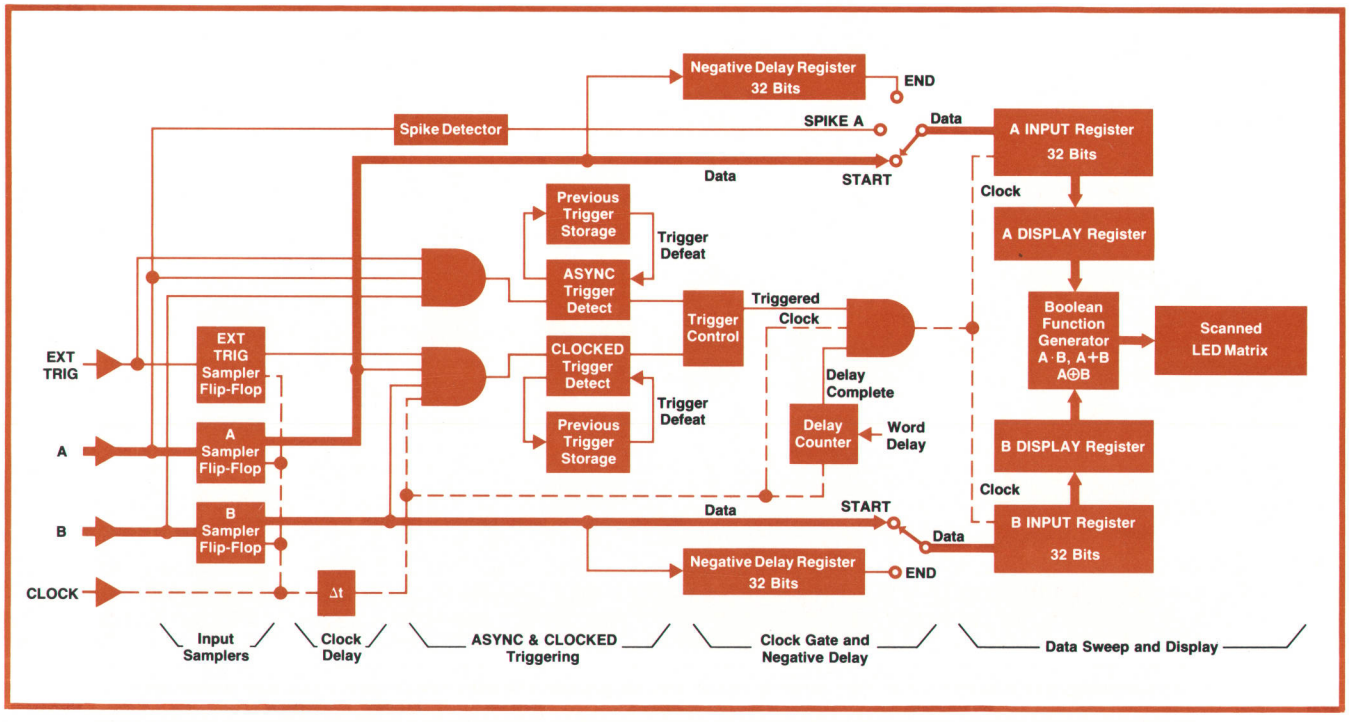


Fig. 9. *Logic Analyzer block diagram.*

Edge sensitivity of the Analyzer's trigger is achieved by an algorithm performed in the blocks labeled "Previous Trigger Storage" in Fig. 9. In words, the algorithm is simply that for a given event to trigger the Analyzer, the previous clock cycle must not have contained a trigger event. Thus the Analyzer does not trigger, for example, if its inputs are such that the front panel AND gate output is continuously HIGH.

In many cases it is desirable to ignore spikes and transients when triggering. This can be done by selecting the CLOCKED mode of operation, in which the inputs are monitored for the trigger condition only at the selected clock edge (Fig. 10). The converse is also possible, in case the desired trigger is a spike. When this happens—that is, trigger information exists only between sampling points—ASYNC mode should be selected. The spike will be captured and stored until the clock occurs to enter it as a trigger condition. Both of these situations are common in digital testing.

Digital Delay Countdown

Once the Analyzer has been triggered, it counts down any digital delay that has been entered in the thumbwheel switch register. The contents of the thumbwheel switches are loaded into six down counters, which are then decremented.

The chain of six down counters may be decremented solely by clock pulses or by a combination of clock pulses and WORD DELAY pulses. When the word delay function is engaged, the left four decades of the thumbwheel switch register are counted down by pulses of lower repetition rate than the clock. These might correspond, for example, to pulses that occur once per serial word in a calculator program. The four digits of word delay in combination with the remaining two digits of clock delay provide coarse and fine digital delays between the trigger and the start of the display.

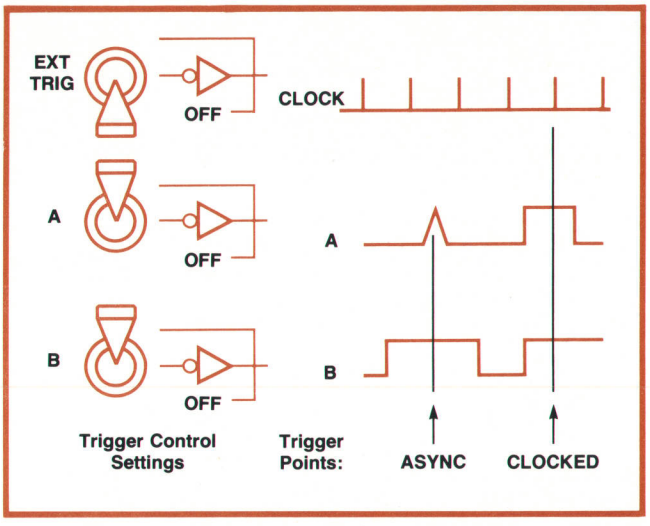


Fig. 10. *In CLOCKED mode, the Logic Analyzer monitors its inputs for the trigger condition only at the selected clock edge. In ASYNC mode, triggering occurs as soon as the trigger condition appears at the inputs. Triggering is always edge-sensitive.*

The Analyzer's negative delay is implemented by running all incoming data through 32-bit digital delay lines (shift registers) prior to loading it into the input registers. When a trigger occurs, therefore, the data that is displayed actually occurred 32 clock periods earlier and has spent the interim traveling through the shift register. The result is a display whose trigger event appears displayed at the right side, or end, of the display. Hence the START and END positions of the DELAY REFERENCE switch.

In END mode the thumbwheels still cause delay in the positive sense. The display ends the indicated number of pulses after the trigger. By selecting the END mode and less than 32 bits of positive delay, pre-trigger and post-trigger events can be seen in the same display.

Display Considerations

In addition to the input registers, which provide the sixty-four bits of information storage, there is also a second set of shift registers that provide an interface to the LED display. The function of these display registers is threefold.

First, the display registers are necessary to position the displayed data bits in the proper place. It was desired that data should always be displayed with the oldest data on the left and the newest data on the right, just as on an oscilloscope display.

The input shift register places each new bit in the rightmost position and pushes older data to the left. Thus if the contents of the input register were displayed directly, data would shift in from the right. To prevent this, as each new bit is entered, the contents of the input register are loaded in parallel into the display register. The display register then quickly shifts so the oldest bit always appears at the left side of the display. This occurs on each clock cycle (Fig. 11). With 32-bit displays, the number of bits that data must be shifted on each clock cycle is thirty two minus the number of bits entered since the start of display.

This data positioning circuitry is required only for low-frequency data, because the movement of data apparent at slow rates cannot be seen above about 1 kHz. Therefore the data positioning circuit is disabled above 1 kHz and data is transferred to the display registers only after all 32 bits of the

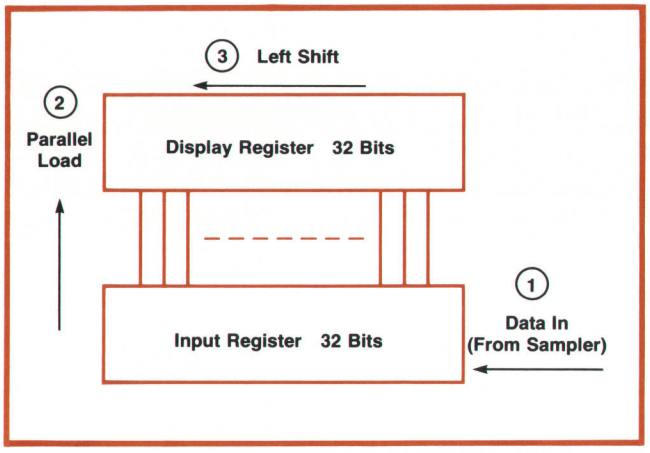


Fig. 11. *Logic Analyzer displays data with oldest information at the left. At clock rates below 1 kHz the three steps shown occur on each clock cycle. The result is that each bit is displayed, properly positioned, as soon as it is entered. Data does not appear to shift in and is viewable while the display is being loaded.*

input register have been reloaded. The advantage is that no high-speed circuitry is needed in the display register.

The second purpose of the display register is to perform the multiplexing function necessary for transferring the data to the scanned display. After the display register is loaded and the data is positioned in the correct orientation, each 32-bit shift register is broken into four eight-bit closed loops. The data in each loop is circulated and one bit of the eight is monitored for the multiplexed data signal. The eight lines corresponding to the eight closed loops of circulating data in the two channels supply the drive (through buffers) to the anodes of the LED's in the 8 × 8 scanned matrix. To properly decode the multiplexed data, the cathodes of the LED's are scanned in synchronism with the shifting of data in the eight-bit loops.

The third function of the display registers is as a source of data to the circuits that perform the Boolean operations (A + B, A • B, A ⊕ B) on the A and B inputs. These Boolean operations take place as the data is scanned into the LED matrix and therefore do not affect the data that is stored in the input registers. This means that any Boolean function can be performed without disturbing the stored data. Thus if it is desired to see this data in its original form it is readily available.

Spike Detection

Selection of the SPIKE A mode makes possible the detection of asynchronous events occurring between clock pulses. A spike is detected whenever more than one logic transition occurs within a single clock period. If the positive-going transition occurs first, the spike is defined as positive and is displayed on the A channel; conversely, negative spikes are displayed on the B channel.

The spike detector consists of two flip-flops (Fig. 12). One is sensitive to the positive-going edge of the data input and the other is sensitive to the negative-going edge. If during any given clock period both flip-flops are set, a spike has occurred. The detected spike is entered into the input register by the next clock pulse.

A positive spike is differentiated from a negative one by a detector and a latch which determine which of the two flip-flops was set first. At the

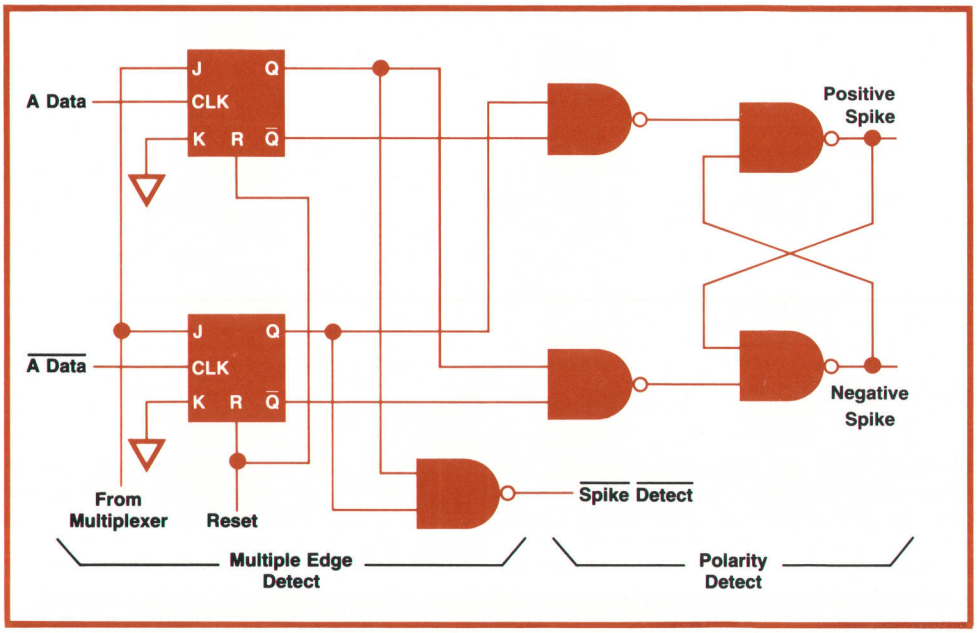


Fig. 12. *Spike detection circuitry detects multiple edges within a clock cycle.*

The IC Troubleshooters

Logic testing needs similar to those for which the 5000A Logic Analyzer was developed had earlier prompted development of a group of handheld instruments that were forerunners of the 5000A. Beginning in 1968 with the now ubiquitous Logic Probe, this family of instruments has grown to include a TTL/DTL Logic Probe, a Logic Clip, a Logic Pulser, a Logic Comparator, and Logic Probes for testing ECL and HTL/MOS circuits.

Logic Probe

The Logic Probe was the first test instrument designed and optimized strictly for digital applications. It has a digital readout, a lamp near the probe tip, that displays logic levels and pulses occurring on the circuit node being probed. The lamp glows brightly to indicate logic HIGH's, goes off for logic LOW's and glows at half brilliance to indicate open circuits or voltages between the preset logic thresholds. Continuous pulse trains cause blinking of the lamp at a 10 Hz rate and single pulses are stretched to provide a visible flash of the lamp: on for HIGH-going pulses and off for LOW-going ones.

Logic Probes are the quickest, surest way of detecting the presence or absence of single or infrequent pulses. No adjustments are needed, and signals can be rapidly traced through circuits by monitoring only two points: the schematic and the probe tip. There is no chance the probe will slip off the intended node while the user turns his head to read a remote display.

The Probe's value derives from the greater speed with which design and troubleshooting faults that result in bad nodes can be found. In these cases the Probe by itself will rapidly isolate the failure. When more detailed analysis is required, such as that of a Logic Analyzer or oscilloscope, the Probe is a useful adjunct. When the user is unable to identify the specific cause of a fault, the Probe can usually localize the search to a small group of suspect IC's and thus more quickly focus the power of the analyzer or oscilloscope on the problem.

The 5 volt probe, Model 10525T for TTL and DTL integrated circuits, has now been joined by two other models. Model 10525E has ECL logic thresholds and a −5.2 volt power input voltage for compatibility with all types of emitter-coupled logic. It's also the fastest of the three probes: pulse detection is guaranteed down to 5 ns. Model 10525H is designed for high voltage logic families such as HTL and HiNIL. A built-in power supply voltage regulator accepts input voltages anywhere between +12 and +25 volts. Logic thresholds are preset to +2.5 volts and +9.5 volts. The "H" probe is also useful with many types of MOS, discrete component, and relay logic systems.

Logic Clip

The second handheld logic tester, introduced in 1970, is Model 10528A Logic Clip. IC's are multi-pin devices, and it's often of interest to see information at several pins at the same time. The Logic Clip was developed to display the logic states of all 14 or 16 pins of a DIP IC simultaneously. The Clip attaches directly to TTL/DTL IC's, automatically seeks the V_{CC} and ground pins, and connects its power and ground buses to the proper pins. The Clip's 16 light-emitting diodes then display the logic states of all pins of the IC, one LED corresponding to each pin. The LED's light to indicate logic HIGH's and remain off for logic LOW's.

The Clip is handy when analyzing sequential circuits such as those containing IC counters or shift regisers. These typically have four or more outputs. With a slow stimulus (about 1 Hz) the progression of logic states can be followed on the Clip. Other applications include monitoring the output states of a ROM or displaying static input-output relationships in combinatorial IC's such as inverters or NAND gates.

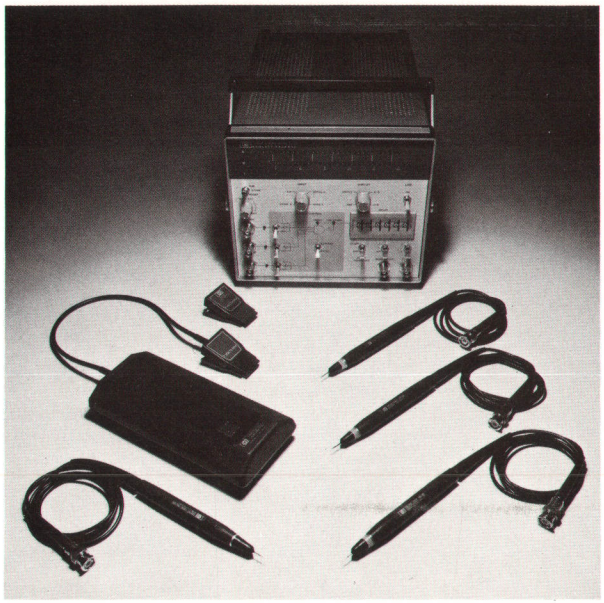
Logic Pulser

The Logic Pulser, Model 10526T, was the fourth of the IC Troubleshooters to be developed. The Probe and Clip are response monitors; they depend on the circuit under test to supply stimulus to IC's while they display the responses. The Logic Pulser contributes in-circuit stimulus, thereby making possible the same kind of stimulus-response testing that has long been invaluable in analog troubleshooting.

The problem of stimulating digital IC's in a circuit is more difficult than it might at first appear. Digital outputs have very low output impedances (less than 5 ohms). They are designed this way to provide wide immunity to spurious noise. Connected in circuits, each relatively high-impedance IC input is driven by a low-impedance output that clamps it either HIGH or LOW at all times. Stimulus is possible by overriding the driving IC output with large amounts of current, but then destruction of the driving stage is a real possibility.

The Logic Pulser solves this problem by generating a very narrow pulse, briefly overriding the driving output. The Pulser will source or sink up to 0.65 amperes each time its pulse button is pressed. Narrow pulse width of 0.3 microseconds, coupled with the manual activation, make the duty cycle very small, so there is negligible added power dissipation in the driving IC and no danger of damage. Automatic selection of the polarity of the output pulse geatly simplifies operation; HIGH nodes are pulsed LOW, and LOW nodes HIGH with no adjustments required.

The Pulser provides stimulus at rates appropriate for moni-



Clockwise from lower left: 10526T Logic Pulser, 10529A Logic Comparator, 10528A Logic Clip, 5000A Logic Analyzer, 10525T Logic Probe, 10525E Logic Probe, 10525H Logic Probe.

toring responses with the Logic Clip. For example, the proper progression of logic states in an IC counter may be verified using Pulser and Clip as a stimulus/response team. The Logic Probe, with its pulse stretcher, is a good companion for the Pulser when testing combinatorial logic such as gates and inverters. The Logic Pulser's 0.3 μs pulse, injected at a gate input, should appear at the gate output and be displayed by the Probe. If it doesn't, the gate is defective.

The Logic Probe, Pulser, and Clip are available in a single package as the 5015T Logic Troubleshooting Kit.

Logic Comparator

The Pulser, Clip and Probe leave most of the task of analyzing results to the user, who must interpret the circuit responses that the instruments display for him. Through his knowledge of circuit operation he decides if his new design is functioning the way he intended or if a particular IC in the instrument he is troubleshooting has failed.

Model 10529A Logic Comparator, an in-circuit IC tester, goes further, analyzing the detected signals to display logical faults rather than HIGH's and LOW's. The comparator functionally tests TTL and DTL IC's in their normal circuit environment without removing them from their printed circuit boards. Failures of the test IC are displayed on the Comparator's 16 LED's, each of which corresponds to a pin of the test device.

The 10529A compares the operation of the test IC to a reference IC of the same type that is inserted in the Comparator. Power and input signals are borrowed from the test IC. Outputs of the two IC's are compared and whenever a logic difference exists the LED corresponding to the differing pin is lighted. Brief or intermittent errors are stretched to provide a visible flash of the LED.

Blank reference boards are supplied with the Comparator, ready for the user to load with the IC's he wants to test. After inserting the IC into the board the user bends power and ground pins to contact the buses that supply the Comparator's power, and solders the IC into place. The user then breaks a trace on the reference board to identify each output pin; this permits the Comparator to differentiate between inputs and outputs. The reference board is then ready for use. An accessory kit of reference boards pre-programmed with 20 commonly used TTL IC's is available.

In a troubleshooting situation, a suspect IC is selected for testing and the corresponding reference board is placed in the Comparator's drawer. The Comparator is then clipped onto the selected test IC and the display is checked for lighted LED's.

The Logic Probe, Pulser, and Clip also complement the Logic Comparator in troubleshooting applications. Many variations are possible. For example, the Probe can be used to isolate the failure to a specific board or group of IC's. Then the Comparator can be brought in to test the smaller number of possibilities. Once a bad node has been located by the Comparator, the Probe and Pulser can analyze the cause. Simultaneously probing and pulsing the suspect node will identify a short to ground or to the power supply: the Pulser can't pulse its own supply buses, so if no signal is registered on the Probe a solder short is likely.

The Pulser is handy when the Comparator is used to test sequential logic. If the reference IC turns on to a different state than the test IC, an error may be indicated. Pulsing the reset input of the test IC synchronizes test and reference IC's to the same state and the test becomes valid. This external synchronization is necessary whenever it is not performed automatically by the circuit or by a manual reset control.

Model 5011T Logic Troubleshooting Kit combines all four TTL and DTL fault-finders: Probe, Clip, Pulser, and Comparator.

References

1. R. Adler and J. Hofland, "Logic Pulser and Probe: A New Digital Troubleshooting Team," Hewlett-Packard Journal, September 1972.
2. M. Baker and J. Pipkin, "Clip and Read Comparator Finds IC Failures," Hewlett-Packard Journal, January 1972.
3. G.B. Gordon, "IC Logic Checkout Simplified," Hewlett-Packard Journal, June 1969.

end of each clock period, the contents of the spike circuit are cleared. To assure that there are no dead times for spike detection, two identical spike detection circuits have been included. Each is active on alternate clock cycles. Thus even when the spike detector is being cleared, a new spike can be detected.

Special Applications

Additional capabilities built into the Logic Analyzer greatly extend its flexibility in certain applications.

First, external access is provided to the data stored in the A and B registers. This data is valuable when using the Analyzer as a serial-to-parallel converter or whenever computer analysis of displayed data is desired. Computer-aided fault isolation in production test is one example.

The top edges of the two register boards that store displayed information are designed to mate with flat-cable connectors. Holes and trace patterns already exist on the boards for IC's to interface the Analyzer's TTL levels to those of other logic families. Layout is for the 7404 pin configuration, and any similar devices (7405, 7407, etc.) may be used to tailor the outputs to specific requirements. Once interface devices are selected and soldered in place, data is available at the connectors at the top of the card. A rear-panel signal, TRIG OUT, functions as the strobing command, signaling with a logic LOW when data is valid.

Second, if it is desired to use the 5000A as a digital trigger and delay generator for an oscilloscope, the 50 ms data hold time (during which the display is frozen) may be reduced to 3μs. To do this one simply moves the programming plug on the Control A board to the TEST position. The Analyzer is then retriggerable 3μs after a display sweep is completed. The 50 ms delay is necessary for proper operation of the Analyzer's display section, so all

displayed information must be ignored with the plug in the TEST position. Data at the top of the register boards, however, is still valid.

Finally, if special triggering capability beyond that provided by the Logic Analyzer is required, inclusion of user-designed add-ons has been facilitated. All necessary data and trigger control signals in addition to +5V power are available at the top of the Trigger Board, which also mates with a card-edge connector. Serial triggering, the ability to trigger when a particular serial bit pattern occurs, could be added in this manner, for example.

Mechanical Design

The 5000A Logic Analyzer is the first instrument to be packaged in the new HP cabinet system. This system features die-cast front and rear frames and removable aluminum side rails that connect the front and rear frames. With top, bottom, and both side covers removed, access to all sides of the instrument is possible (Fig. 13). The covers slide into slots on the frame; each is quickly removed by loosening only a single screw.

The internal design of the Logic Analyzer emphasizes ease of assembly from both manufacturing and service viewpoints. Its chassis is a single printed-circuit mother board containing a series of card-edge connectors. All electronic components are mounted on printed-circuit modules that plug into the mother board, which contains all interassembly connections. The printed-circuit modules are easily extendible or removable for troubleshooting purposes, and hand wiring is kept to a minimum. Even the front and rear-panel controls are printed-circuit mounted; the only hand wiring in the instrument is the IEC-required power and transformer wiring.

The Logic Analyzer cabinet is a standard half-rack module, 15 inches deep. Its handle, 15 pound weight, and form factor make it light and convenient to carry (Fig. 14).

Acknowledgments

The authors wish to acknowledge the following people whose help was greatly appreciated throughout the design and production introduction phases: Jim Marrocco for mechanical design, Jack Nilsson for his inputs on serviceability, Chuck Taubman and Gary Gordon for their guidance and management, Roy Criswell for a smooth, on-time production introduction, and Jesse Pipkin for his constant efforts to configure an instrument in concert with market needs.

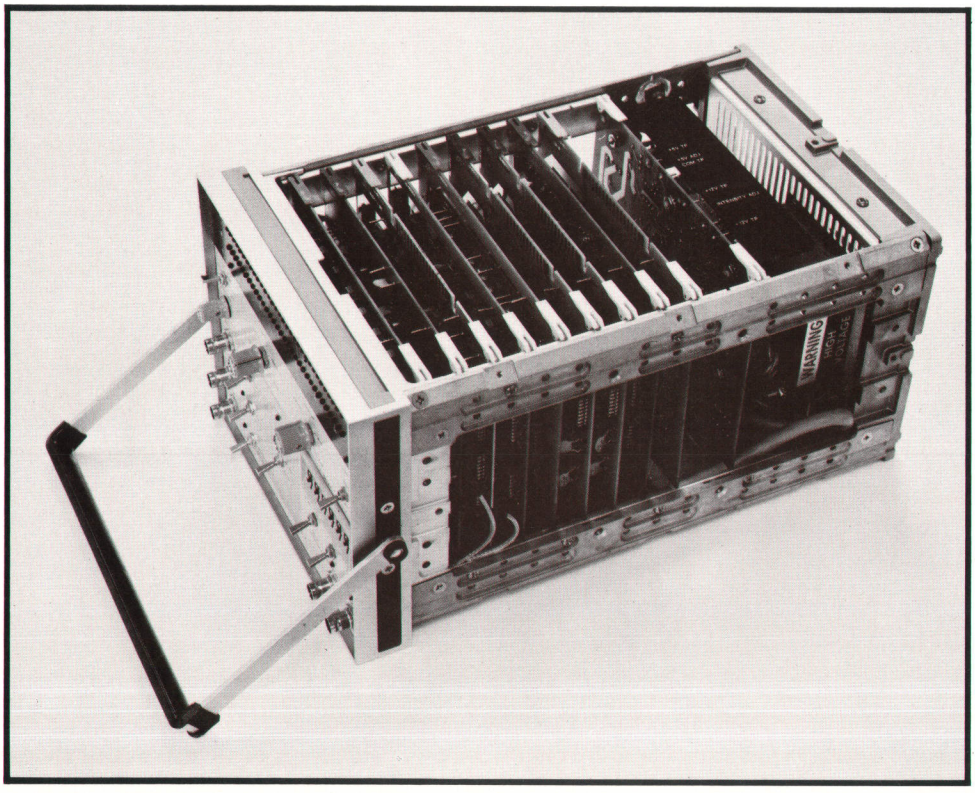
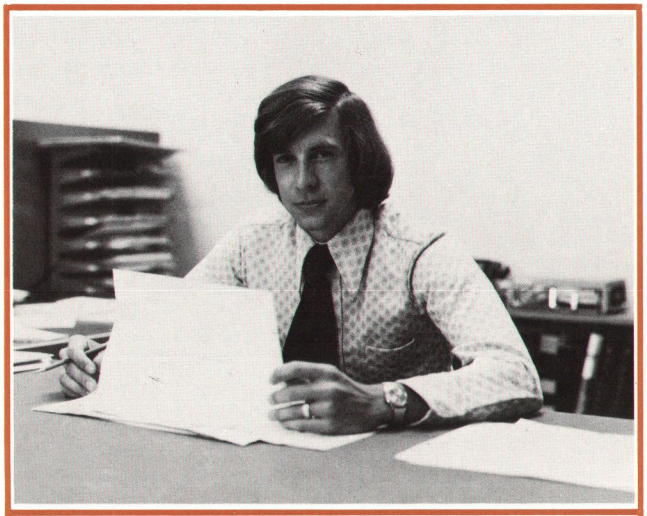


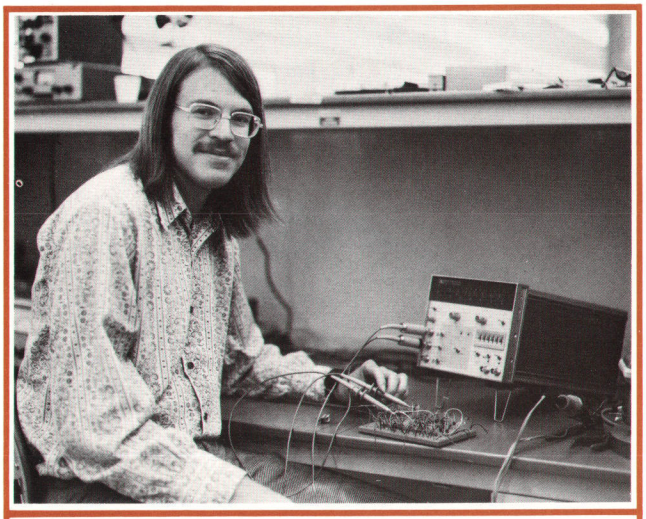
Fig. 13. *Logic Analyzer is mechanically designed for ease of assembly and repair. Top, bottom, and sides are easily removed to gain access to all sides of the instrument.*



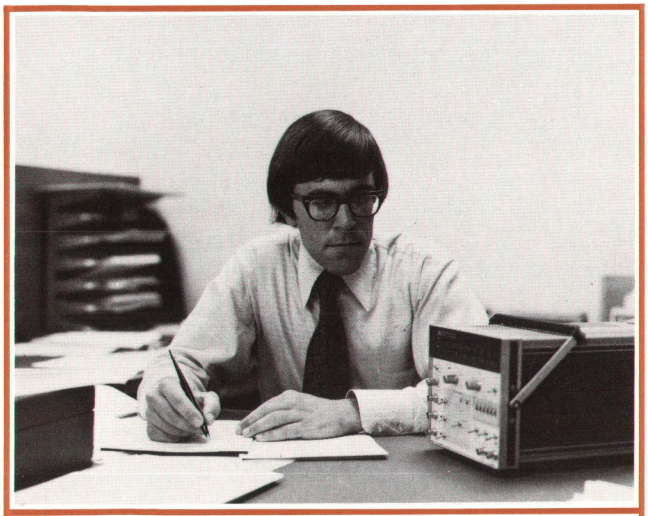
Fig. 14. *Light weight, handle, and form factor make the Logic Analyzer suitable for field service applications.*



Mark Baker
Logic test product marketing engineer Mark Baker assumed his present position after serving as engineering project leader for the 5000A Logic Analyzer. A native of Oklahoma, Mark received his BS degree in electrical engineering from Oklahoma State University in 1969 and his MSEE degree from Stanford University in 1970. His first product for HP was the 10528A Logic Clip, which he designed during the summer of 1969. He's also contributed to the design of the 5525A Laser Interferometer and the 10529A Logic Comparator. For recreation, Mark likes water skiing, tennis, and tinkering with cars. He and his wife live in Cupertino, California.



Howard D. Marshall
Howard Marshall received his BS degree in engineering from California Institute of Technology in 1970, and came to HP the same year. After a brief exploration into high-speed test systems, he helped invent the 10526T Logic Pulser and made major contributions to the design of the 5000A Logic Analyzer. He's now a project leader in the logic test laboratory. A native of Nampa, Idaho who now lives in Woodside, California, Howard enjoys backpacking, bicycling, and making his own wine.



Robin Adler
Robin Adler joined HP in 1970 after receiving his BS degree in electrical engineering from California Institute of technology. After two years of digital design he became project leader for the 10526T Logic Pulser. When that project was completed in 1972 he moved into logic test marketing and now has marketing responsibility for the 5000A Logic Analyzer. Robin spends a good deal of his spare time restoring old cars, mostly foreign ones. Weekends and vacations he's likely to spend in the mountains, camping or skiing, depending on the season.

SPECIFICATIONS

HP Model 5000A Logic Analyzer

Inputs

NUMBER: 5 (Channel A, Channel B, External Trigger, Word Delay, Clock).

INPUT IMPEDANCE: 1 MΩ shunted by approximately 25 pF.

INPUT THRESHOLD VOLTAGE: Continuously variable over ±1.4 V (±14 V with 10:1 divider probe).

MAXIMUM INPUT VOLTAGE: ±200 V continuous, ±400 V transient.

ANNUNCIATORS: One per input to display logic state; pulse stretching for single pulses.

DATA AND TRIGGER INPUTS (Channel A, B, External Trigger)
- MINIMUM SETUP TIME: 15 ns (8 ns typical).
- MINIMUM HOLD TIME: 0 ns.

CLOCK INPUT
- MAXIMUM PULSE REPETITION RATE: 10 MHz.
- MINIMUM PULSE WIDTH: 15 ns (10 ns typical with 100 mV overdrive).
- HYSTERESIS: Approximately 10 mV.

WORD DELAY INPUT
- MAXIMUM PULSE REPETITION RATE: ½ of Clock input repetition rate (input is synchronized to Clock).
- MINIMUM PULSE WIDTH: 15 ns.
- WORD DELAY SLOPE CONTROL SWITCH: Permits selection of high or low-going edges of word pulse or disabling of function.

Input Modes

A, B: Two-channel operation.

SERIAL A: A and B display registers cascaded into a single 64-bit display loaded from Channel A input.

SPIKE A: Detects multiple transitions at A input during a clock period. Positive spikes are displayed in A display register, negative spikes in B register.
- MINIMUM SPIKE WIDTH: 15 ns (10 ns typical with 100 mV overdrive).

RUN-STORE-RESET MODES
- RUN: Normal operation, A and B registers loaded each time Analyzer triggers.
- STORE: Analyzer triggers once (or finishes current sweep) and retains data, rearming inhibited.
- RESET: Clears A and B display registers (except in Store B mode) and rearms Analyzer when released. Also aborts sweep or delay countdown if in progress.

STORE B MODE: Data in Channel B display register is retained (sweep is completed if in progress). Channel A loads each time Analyzer triggers. Reset control does not affect data stored in B register.

Trigger Controls

FUNCTION: Initiate display or delay countdown (also see Digital Delay section).

ARMING: Analyzer must be armed in order to trigger. Arm LED lights to indicate arming.
- MINIMUM SWEEP REARMING TIME: Approximately 50 ms after last clock pulse of sweep.
- HOLDOFF CONTROL: Increases rearming time up to approximately 5 seconds.

TRIGGER CONDITIONS: Triggering may be from either Data input, External Trigger input, or logical AND combinations of two or three inputs. Slope selection is provided by 3-position slope control switch for each input.

TRIGGER SLOPE CONTROL SWITCHES
- SWITCH UP: Input must be HIGH for triggering.
- SWITCH IN CENTER POSITION: Input must be LOW for triggering.
- SWITCH DOWN: Input does not affect triggering.

TRIGGERING MODES
- CLOCKED MODE: Analyzer triggers on first clock pulse after all input conditions defined by slope control switches are met. Trigger condition must remain until clock pulse occurs.
- ASYNCHRONOUS MODE: Analyzer triggers when trigger conditions are met. Conditions need not remain until clock pulse occurs.
- MINIMUM PULSE WIDTH: 40 ns.
- MINIMUM SETUP TIME: 60 ns.

TRIGGER LED: Indicates Analyzer is triggered. Remains on until completion of sweep.

Digital Delay

POST-TRIGGER DELAY RANGE: Display begins 0 to 999,999 clock periods after trigger event.

PRETRIGGER (NEGATIVE) DELAY RANGE: Display begins 0 to 32 clock periods (64 in Serial A mode) before trigger event.

WORD DELAY: When enabled, permits 2 levels of digital delay.
- DELAY RANGE: 0 to 9,999 pulses at Word Delay input plus 0 to 99 pulses at Clock input.

Display

TYPE: Red light-emitting diodes.

LENGTH: 32 LED's per register.

LOGIC CONVENTION
- ON LED: Logic HIGH (input more positive than threshold voltage).
- OFF LED: Logic LOW (input less positive than threshold voltage).

DISPLAY MODES
- DIRECT: Data at A and B inputs displayed by A and B registers.
- A • B: Logical AND of A and B inputs displayed in A register, B register blanked.
- A + B: Logical OR of A and B inputs displayed in A register, B register blanked.
- A ⊕ B: Logical EXCLUSIVE-OR of A and B inputs displayed in A register, B register blanked.

DISPLAY RELATIONSHIP TO CLOCK: Display advances horizontally one LED per clock pulse.

Rear Panel

THRESHOLD ADJUSTMENT
- THRESHOLD RANGE SWITCH: Selects low range (approximately −0.14 to +0.14 V) or high range (approximately −1.4 to +1.4 V) for input amplifier threshold voltage.
- VERNIER CONTROLS: Permit continuous adjustment over either range.
- THRESHOLD OUTPUT: Enables measurement of threshold voltage, $Z_0 \simeq 5.6\ k\Omega$.

TRIGGER OUT: Goes HIGH when delay countdown is completed; remains HIGH until display sweep has completed.

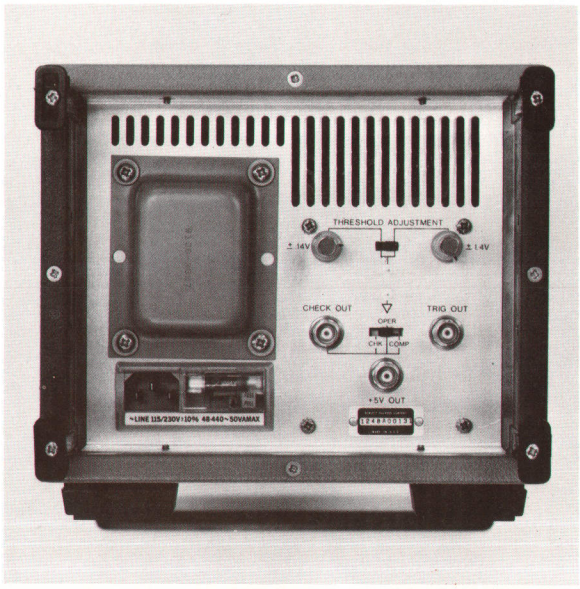
5 V OUT: Supplies 5 V ±5% at 200 mA.

CHECK-OPERATE-COMPENSATE
- CHK: Provides alternating HIGH/LOW display when Check Out output is connected to Channel A or B input. No external clock required.
- OPER: Normal Analyzer operation.
- COMP: Used for adjusting compensation of divider probes.

CHECK OUT: Provides signal at ½ clock input repetition rate (except in Check mode); TTL compatible.

PRICE IN U.S.A.: $1900.00

MANUFACTURING DIVISION: SANTA CLARA DIVISION
5301 Stevens Creek Boulevard
Santa Clara, California 95050 U.S.A.



A Pulse Generator for Today's Digital Circuits

This new dual-output Pulse Generator produces 16V pulses at high repetition rates, and with as much as 16V offset. A new control arrangement makes pulse set-up much simpler.

by Reinhard Falke and Horst Link

BECAUSE OF THE rapidly expanding role that digital circuits play in present-day technology, pulse generators introduced recently by Hewlett-Packard were designed to drive integrated circuits. The main emphasis with these instruments was to provide high repetition rates, 50 MHz and higher, as well as to produce well-defined pulse shapes. Intended as test signal sources for TTL and ECL circuits, these instruments had maximum output levels of ±5 V (into 50Ω) with a baseline offset range of ±2 V or so.

MOS integrated circuits and high-threshold "noise immune" circuits, however, require higher voltage levels. Accordingly, a new dual-output pulse generator (Fig. 1) has been designed with a capability for supplying pulse amplitudes up to 16 V into a 50Ω load from a 1kΩ source impedance, or 8 V into 50Ω from a matched 50Ω source. Not only are these drive levels suitable for testing CMOS, N-channel MOS and most high-threshold MOS circuits, as well as TTL and other digital circuits, but they are also useful as test signals for examining the transient response of operational amplifiers, oscilloscopes, and other wideband analog circuits. In addition, the two output channels can be combined to supply twice the single-channel

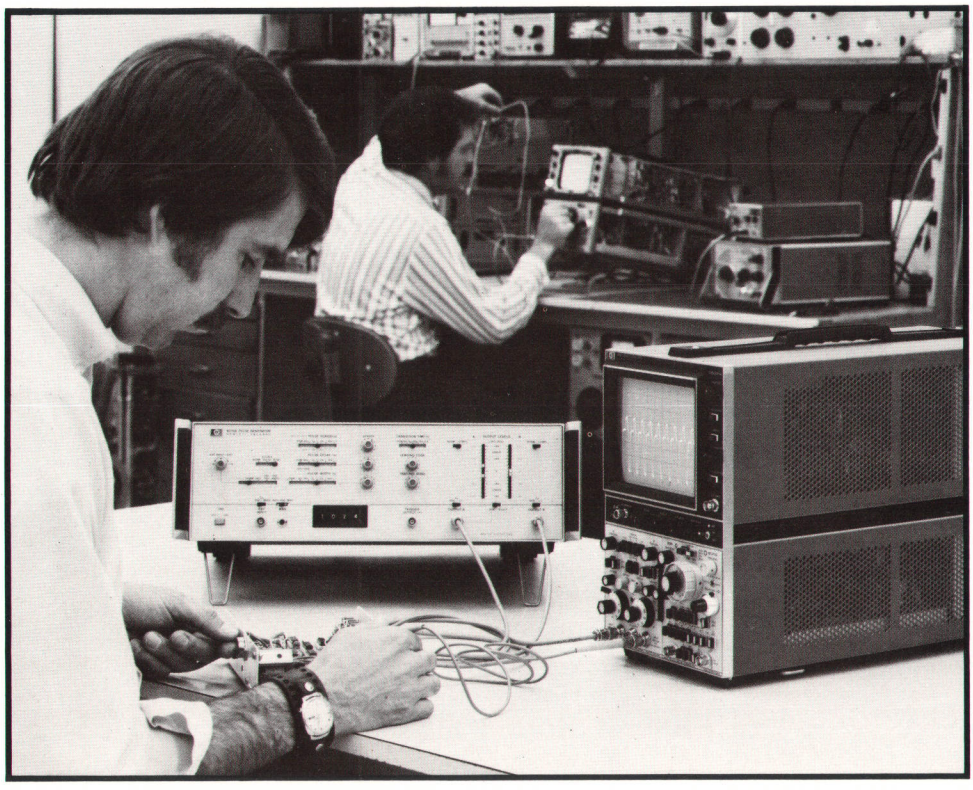


Fig. 1. *New Model 8015A 50 MHz Pulse Generator has two outputs with individual control of amplitude, polarity, and baseline level for each. The arrangement of the controls simplifies operation. The instrument shown here is equipped with the optional burst mode of operation.*

output current, especially useful when the generator is used to drive magnetic devices. The doubled current capability enables pulse swings of up to 30 V anywhere within a +16 V to −16 V window.

The maximum repetition rate of this instrument depends on the pulse amplitude selected (and, of course, on the characteristics of the load). With the internal 50Ω source impedance switched in, the repetition rate can go as high as 50 MHz up to the maximum amplitude (8 V) obtainable in this mode. Without the internal 50Ω, pulses up to 16 V can be generated at repetition rates up to 40 MHz.

Two-Phase Generation

With its two output channels the new pulse generator (Model 8015A) can supply the two-phase clock signals needed by many MOS circuits. Pulses in the B output channel can be delayed with respect to pulses in the A channel, the time delay being set by the PULSE DELAY controls (Fig. 2). Pulses from both channels will have the same width and transition times, but their output levels and polarities are individually selectable.

The controllable delay between channels is also useful for testing coincident gates and the set-reset characteristics of flip-flops.

Simplified Output Control

Setting the output levels of this instrument has been made much easier by a new control arrangement. The usual method of setting output levels has been to use an uncalibrated offset control to set the baseline and to adjust pulse amplitude with the output attenuator and vernier control. A precision oscilloscope was therefore needed to determine the levels of the baseline and pulse top exactly.

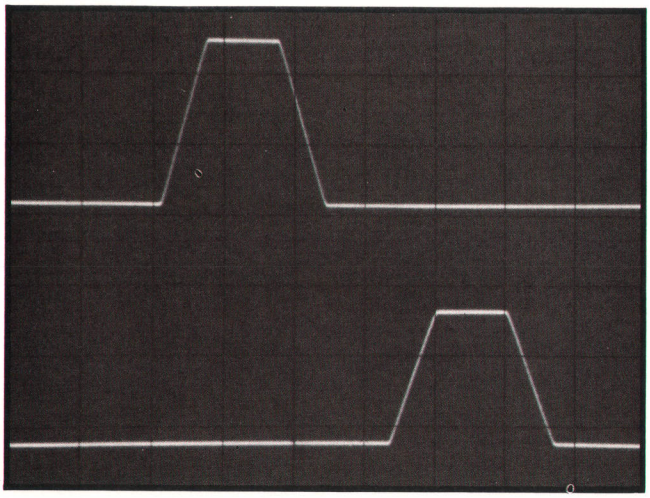


Fig. 2. *Dual-trace oscillogram shows how pulses in channel B can be delayed with respect to channel A, giving two-phase clock pulses.*

Output levels of the new pulse generator are determined by calibrated dual-slider controls (see Fig. 3). The lower slider sets the baseline and the upper slider sets the level of the pulse top. Transition times are not affected and remain constant through all settings of these controls. When the output is switched to the complementary mode, the pulse is inverted but the upper control continues to set the upper waveform level and the lower control sets the lower level. The sliders are mechanically interlocked so when the maximum pulse amplitude is reached (16 V), further movement of either slider causes the other to follow.

When the output switch is set to A+B, internal switching parallels the outputs of both channels to give a maximum pulse current of 640 mA, twice the normal output. Pulse levels are then controlled by the channel A output level sliders (within the permissible ±16 V "window"). The maximum repetition rate in this mode of operation, however, is limited to 20 MHz because of the greater transition times incurred (minimum = 15 ns).

If the instrument is switched to the B-delayed mode while in the A+B mode, three-level signals can be obtained (Fig. 4). Then the channel B level and polarity controls operate independently of channel A.

Burst Option

The burst mode, an optional feature, will be of particular interest to those who work with shift registers, memories, and logic circuits in general. With this feature, the generator can be set to produce a predetermined number of pulses, then stop. The operator can then check the states of his logic circuits and, since he knows exactly how many pulses were fed in, verify that the circuit is operating properly.

The number of pulses in the burst is selected in a range of 1 to 9999 by the front-panel thumbwheel switch (see Fig. 3). On receipt of a trigger from an external source or from the front-panel pushbutton, the instrument starts generating pulses and an internal counter counts them. When the exact number of pulses has been counted, the instrument stops. Unlike the conventional gate mode of operation, the number of pulses in the burst remains constant, even though the repetition rate may be changed, and it is unaffected by drift in the rate generator and/or gating pulse.

Front-End Similarities

In other respects, the new Model 8015A is similar to other high-repetition-rate generators in the Hewlett-Packard 8000-series (Models 8007A, 8008A, 8012A, 8013A). It has an internal wide-range rate

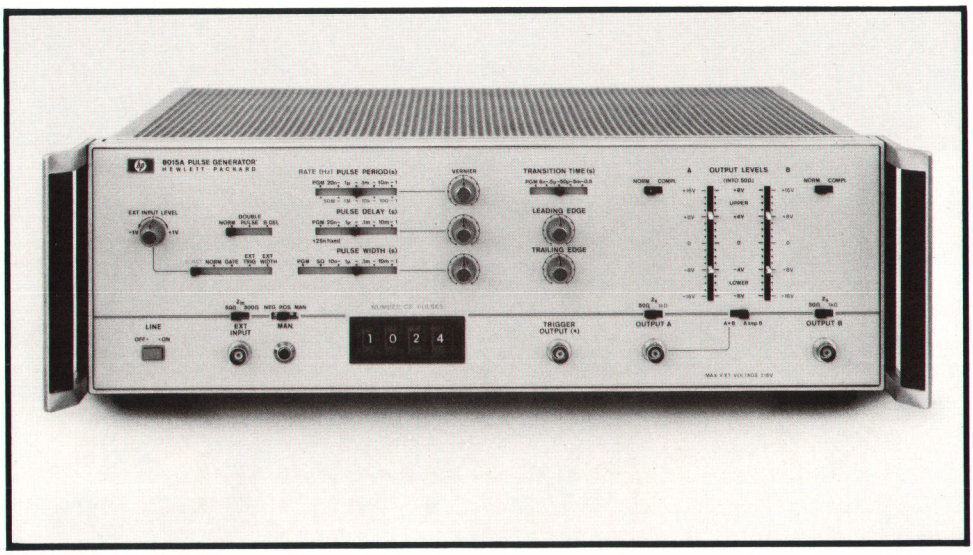


Fig. 3. *Output levels are set by calibrated linear controls. The upper slider sets the upper pulse excursion and the lower slider establishes the lower excursion. The center scale is used when Z_s switches are set to 50Ω while driving 50Ω loads. The outside scales are used when driving either high-impedance loads with Z_s set to 50Ω, or a 50Ω load with Z_s set to 1kΩ. Controls provide visual indication of compatible settings. As long as the PULSE DELAY and WIDTH controls are to the left of the PULSE PERIOD control, there is no danger that the width or delay settings would exceed the pulse period.*

generator (1 Hz–50 MHz) and it also works with external triggers. In addition, it generates a single pulse each time a front-panel pushbutton is pressed.

Pulse width is selectable in a range of 10 ns–1 s with controls that are arranged to make incompatible settings unlikely, e.g. pulse width wider than pulse period (Fig. 3). The instrument also functions in a square-wave mode in which the pulse width is always 50% of the pulse period even though the repetition rate may be changed. This mode is useful for toggle-rate testing of flip-flops, or for applications requiring constant signal power.

A DELAY control, with a range of 25 ns to 1 s, establishes the time interval between a trigger pulse output and the main pulse. This control is also used in the B-delay mode, described previously, to set the time delay between the A and B channels.

The DELAY control is also used in the double-pulse mode. In this mode, useful for checking the pulse resolution of counting circuits, two pulses are generated sequentially in response to each trigger. The DELAY control sets the time interval between the two pulses. The gate and burst modes, incidentally, can be used with both the double-pulse and B-delay modes (maximum repetition rate in these modes is 25 MHz).

The instrument has the conventional synchronous gate mode, where the rate generator is enabled by the presence of a signal at the EXTERNAL input or by the manual pushbutton being pressed. The rate generator remains enabled as long as the signal is present or the pushbutton is held down. Otherwise it turns off. The first pulse is always synchronized with the leading edge of the input signal and the last pulse (or last pair of pulses in the double-pulse mode) is always completed even though the input may turn off while a pulse is being generated.

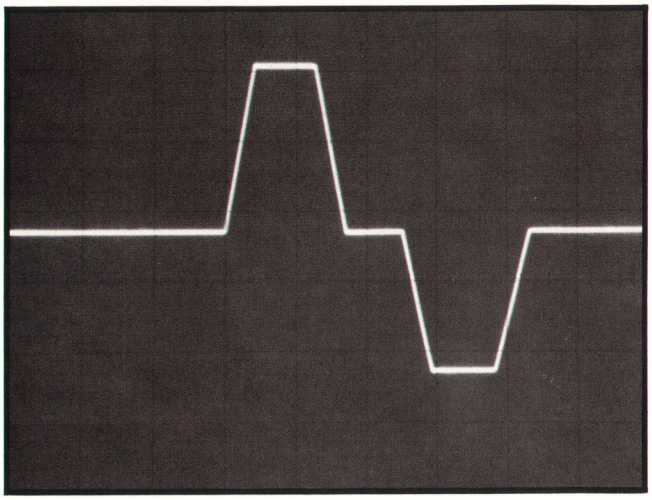


Fig. 4. *Three-level signals are obtained by combining outputs (A+B) while using the B-delay mode. Pulse amplitude and polarity are individually adjustable but pulse widths and transition times are identical and are adjusted simultaneously (pulses cannot be overlapped).*

Controllable Transition Times

The rise and fall transition times of the output pulses can be controlled within a range of <6 ns to 500 ms. Controlled transition times are useful for testing devices such as core memories, where the device response is affected by transition time, and for simulating propagation degradation in long cables. It is also useful for confirming propagation delay in acceptance testing of digital circuits since IC manufacturers include risetime of the test pulse as part of the specification.

Transition times are selected by a range switch, common to both rise and fall times, and separate verniers for rise and fall. Within each range, transition times are adjustable over a 100:1 span.

Pulse Regeneration

The new instrument also has a "width" mode. In this mode, pulses applied to the EXTERNAL input bypass the rate generator, width, and delay circuits, going directly to the pulse-shaping circuits. The output pulses then have the same width as the input, but with controllable levels and transition times. The instrument thus serves as a pulse regenerator, shaper, or amplifier for waveforms of any shape generated elsewhere—the output stays "on" as long as the input signal stays above the trigger level, and drops back to the baseline whenever the input falls below the trigger level. This mode is useful when working with a word generator, for example, when the word generator does not have the output capabilities needed for the task at hand.

Theory of Operation

A block diagram of the Model 8015A Pulse Generator is shown in Fig. 5. Triggers for the pulse-generating circuits are produced by the rate generator, a solid-state relaxation oscillator that uses an RC charging circuit to establish the basic pulse period.

When external signals or the front-panel pushbutton are used to trigger pulse generation, the RC timing circuit is disconnected and the oscillator RC discharge switch then functions as a pulse driver for the succeeding circuits. The switch is driven by pulses formed in the signal conditioning circuits, which have the same kind of polarity and level selection as oscilloscope time bases.

In the gate mode of operation, the signal conditioner works as a Schmitt trigger to generate rectangular pulses with widths equal to the times that the external signal remains above the selected triggering level. The rate generator then oscillates as long as the input is above the triggering level, but otherwise oscillations are suppressed. As in the NORM mode of operation, pulse repetition rate during the "on" time is determined by the front-panel RATE (PULSE PERIOD) control.

In the optional burst mode, the rate generator enable/disable function is performed by the burst control circuit. On receipt of a trigger (either external or manual), the burst circuit loads the number that has been set into the front-panel thumbwheel switches into a counter, and it enables the rate generator. Each of the rate generator pulses decrements the counter one count, counting down to zero. A digital detector senses the all-zero state of the counter and then disables the rate generator, terminating the burst.

The rate generator supplies triggers to the front-panel TRIGGER output and it also drives the delay generator. This is a monostable circuit that turns "on" in response to a rate generator trigger and turns "off" again at a time determined by the front-panel PULSE DELAY controls. The trailing edge is used as a trigger for the width generator so the main output pulse is delayed with respect to the front-panel output triggers.

In the double-pulse and B-delayed modes, triggers are derived from both the leading and trailing edges of the delay monostable pulse. Consequently, two output pulses are generated for each input trigger—one pulse at the same time as the trigger, and the other occurring later at a time determined by the delay setting.

The width generator is another monostable circuit that turns "on" for a time determined by the front-panel PULSE WIDTH controls. The rectangular pulse thus generated is passed on to the pulse-shaping circuits.

Square Waves

In the square-wave mode, the rate generator output goes to a flip-flop that generates a square wave

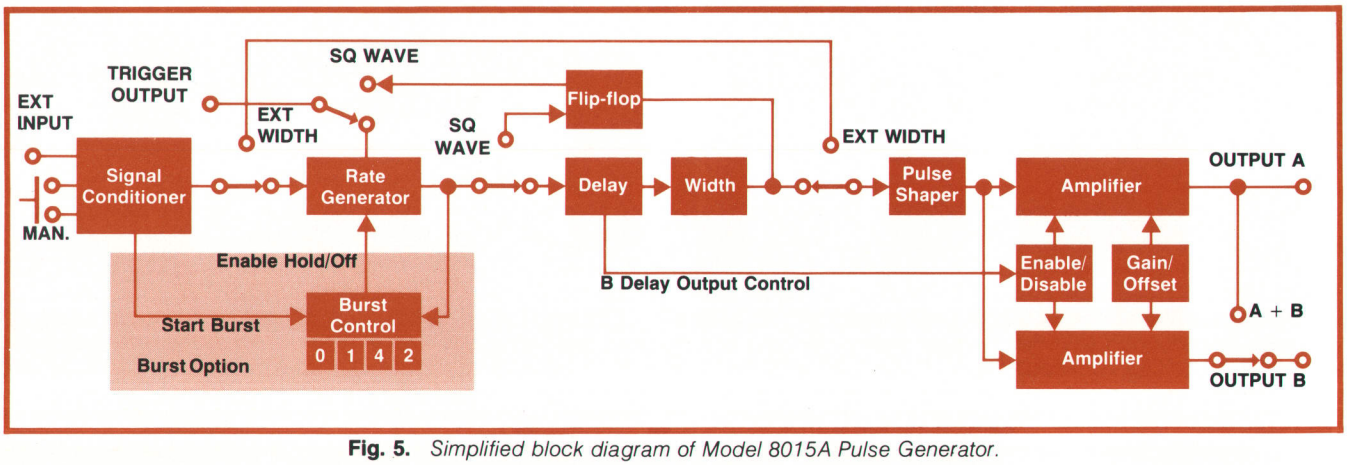


Fig. 5. *Simplified block diagram of Model 8015A Pulse Generator.*

with a repetition rate one-half that of the rate generator. The flip-flop also generates triggers at the half rate. This square wave goes directly to the pulse-shaping circuits, bypassing the delay and width circuits.

The square-wave function can also be used with the gate and burst modes but in this case, the number of square-wave cycles in the burst is only one-half the number of triggers counted. Accordingly, to return the output at the end of the burst to the same level as the start, the gate or burst should be set so that an even number of triggers is counted.

Transition-Time Control

The pulse shaper consists essentially of two switched current sources and two clamps. On a positive-going transition, the "positive" current source is switched on, linearly charging a capacitor. When the capacitor voltage reaches the upper clamp level, the clamp absorbs the output of the current source, preventing any further charge of the capacitor. The current magnitude is adjustable so the slope of the transition can be varied.

On a negative-going transition, the "positive" current source switches off and the "negative" current source switches on. The capacitor then charges in the opposite direction until its voltage reaches the lower clamp level where it remains until the next positive-going transition. The result is a trapezoidal-shaped waveform.

The upper and lower current sources are adjustable separately over a 100:1 range, so the slopes of the leading and trailing edges can be adjusted individually. The range of adjustment is determined by the capacitor, which can be changed by the front-panel TRANSITION TIME range switch.

Because of the relatively large amplitude of the pulses generated by this instrument, the speed of the fastest transition is limited by the output circuits, and this limit depends on the output configuration and the nature of the load. The fastest transition (<6 ns) is obtained when driving a 50Ω load with the 50Ω internal source impedance switched in. With the 1kΩ internal source impedance, the fastest transition is 8 ns into a 50Ω load. In the A+B mode, fastest transition is 15 ns with or without the internal 50Ω. With loads other than a well-matched 50Ω, the maximum speed attainable depends on the load capacitance.

Output Stages

At first glance it would seem that control of the output levels could be a simple matter of using adjustable clamp circuits, one to set the baseline level and the other to set the pulse top. This method is not applicable, however, because the transition times would not remain constant as either clamp level were changed.

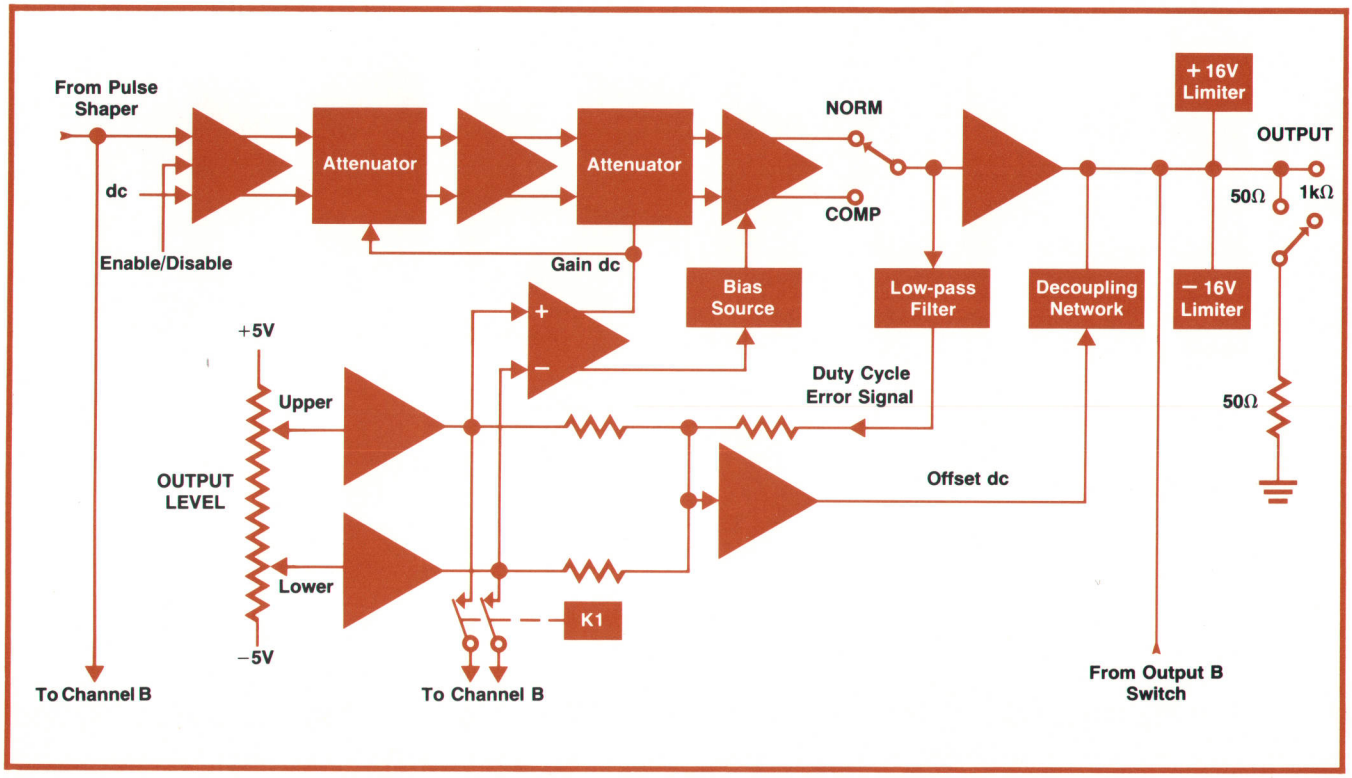


Fig. 6. *Output stages for Channel A. Channel B is identical.*

Actually, the operation of the Model 8015A's output amplifier is similar to earlier pulse generators: peak-to-peak amplitude is determined by amplifier gain and the baseline is set by a dc offset voltage added to the output waveform.

As shown in Fig. 6, the pulse upper and lower levels are selected by sliders on the OUTPUT LEVEL potentiometer. The *difference* between the slider voltages is used to control pulse amplitude, since the peak-to-peak amplitude is proportional to this difference. The *sum* of the slider voltages is used to generate a current that is proportional to the desired offset. This is added to the pulse waveform at the output through a decoupling network that prevents the capacitance of the offset circuits from slowing the pulse transition times.

This method of setting pulse levels requires electronic control of the pulse amplitude. Accordingly, active attenuators[1] of the type shown in Fig. 7 are used. One pair of these attenuators, in a push-pull configuration, is used between stages 1 and 2 of the output chain (Fig. 6) and a second pair is between stages 2 and 3. Each attenuator has a range of 2.75 to 1, giving an overall attenuation range of about 8 to 1.

The difference voltage also adjusts the bias levels of the third amplifier stage so the pulses will be centered in the linear range of this amplifier regardless of amplitude.

Complementary Output

The NORM/COMP switch selects either the noninverted or the inverted output of the differential amplifier chain for presentation to the power output stage.

The output stage normally has a source impedance of 1kΩ. A 50Ω source impedance is obtained by switching in a 50Ω resistor. This absorbs any signal reflections from impedance mismatches in the external system so there will be no re-reflections to distort the primary pulse. When reflections are not a problem, maximum signal drive can be obtained by switching out the 50Ω.

Delayed Pulses

In the B-delayed mode, an enable/disable circuit is activated under control of the pulse delay generator. When the delay monostable circuit is "on," the channel B output amplifier is disabled, so the first pulse appears only in the channel A output. When the delay monostable goes "off," channel A is disabled and channel B is then enabled. In effect, the instrument is functioning in the double-pulse mode, but the first pulse of each pair is processed through channel A and the second pulse goes through channel B.

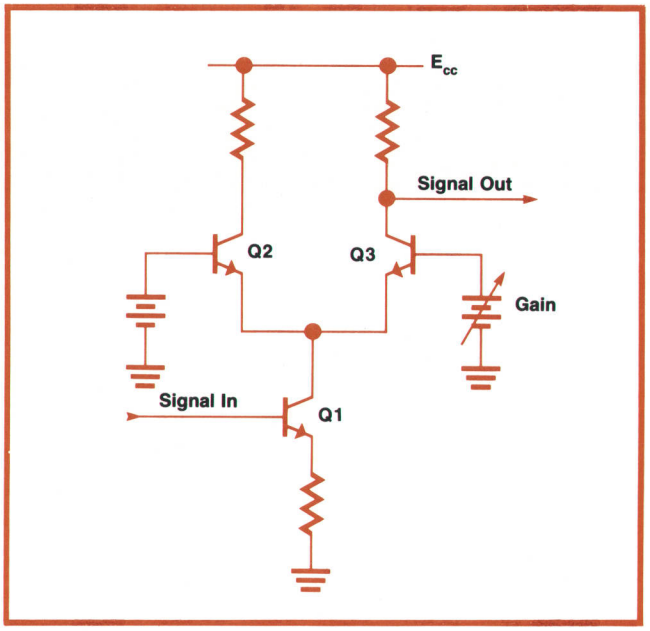


Fig. 7. *Electronic attenuator splits the signal current into two paths. The proportion that goes to Q3 depends on Q3 bias. Q2 sinks the remainder.*

Combined Outputs

In the A+B mode, the switch in the channel B output places the outputs in parallel and relay K1 gives control of pulse levels in both channels to the channel A OUTPUT LEVEL controls. To prevent both source impedance resistors from being placed in parallel, the channel A 50Ω source impedance resistor is automatically disconnected so output impedance is established by the channel B switch.

When the B-delayed mode is used at the same time as A+B, the outputs are in parallel but K1 is opened. The two pulses generated separately in channels A and B are then combined at the channel A output. It should be noted that the offsets are added too, so the pulse baseline will be at a level corresponding to the algebraic sum of the output level sliders that set the baseline in each channel.

Acknowledgments

Among those who worked on the design of the Model 8015A Pulse Generator, and who deserve special thanks for their contributions, are Winfred Freihoff, Theo Papatheodorou, Michael Wollgast, Gert Globas, and Günter Zieher (Pulse Generator Group Leader).

References

1. J. Riggen and D. Fogg, 'An Agile Graphic Display Device,' Hewlett-Packard Journal, April 1972.

SPECIFICATIONS

HP Model 8015A Pulse Generator

Pulse Characteristics

TRANSITION TIMES: From minimum (see Table) to 0.5 s in four ranges. Ranges are common for both transitions with leading-to-trailing edge ratios within each range continuously variable from 100:1 to 1:100.

TRANSITION LINEARITY: For transition times >30 ns, deviation from straight line between 10% and 90% points is less than 5% of pulse amplitude.

OVERSHOOT AND RINGING: ±5% of pulse amplitude, possibly increasing to <±10% at minimum amplitude.

PRE-SHOOT: <5% of pulse amplitude.

PULSE TOP DROOP: <5% of pulse amplitude.

PULSE WIDTH: <10 ns to 1 s in four ranges. Vernier provides continuous adjustment within each range.
WIDTH JITTER: <0.1% + 50 ps.

MAX DUTY CYCLE: >75% from 1 Hz to 1 MHz, decreasing to 50% at 50 MHz. Switching output to COMP mode gives equivalent of 50 to 100% duty cycle.

SQUARE WAVE SYMMETRY: ±5% from 1 Hz to 1 MHz, going to ±15% at 25 MHz (internal modes only).

PULSE DELAY: 20 ns (+25 ns fixed) to 1 s with respect to trigger output. Four ranges with vernier for continuous adjustment within each range.
DELAY JITTER: <0.1% + 50 ps.

PULSE OUTPUTS: Two outputs with independent control of pulse upper and lower levels, source impedance, and normal or complemented output (see Table).
A + B: Output channels combined through channel A output (with no load connected to channel B output). In NORM and DOUBLE PULSE modes, pulse levels and norm/complement selection are controlled by channel A (channel B controls are disabled). In B DELAY mode, both channel A and channel B controls are enabled for independent control of first and second pulses in each pair. Output levels in each part of combined waveform then equal algebraic sum of channel A and channel B levels.

Repetition Rate and Trigger

REPETITION RATE: 1 Hz to 50 MHz (see Table) in four ranges. Vernier provides continuous adjustment within each range.
PERIOD JITTER: <0.1% + 50 ps.

SQUARE WAVE: 0.5 Hz to 25 MHz (½ of repetition rate).

DOUBLE PULSE: 1 Hz to 25 MHz. Spacing between pulses in each pair defined by delay controls.

B DELAY: 1 Hz to 25 MHz. Channel B pulse delayed with respect to channel A pulse, as defined by delay controls.

TRIGGER OUTPUT: >1 V into 50Ω load, dc coupled. 50Ω typical source impedance.
TRIGGER PULSE WIDTH: 9 ns ± 5 ns.

Externally-Controlled Operation

REPETITION RATE: 0 to 50 MHz. For square-wave output, ½ of repetition rate.

TRIGGERING:

INPUT IMPEDANCE (switched)	50Ω	500Ω
SENSITIVITY Sinewaves Pulses	 1 V p-p ±0.5 V	 10 V p-p ±5 V
THRESHOLD (Continuously adjustable)	−1 to +1 V	−10 to +10 V
POLARITY (switched)	Positive or negative slope	
MAXIMUM INPUT	±7 V	± 25 V

DELAY: <50 ns between input and output triggers.

MANUAL: Front-panel pushbutton generates one input trigger each time it is pressed.

GATE MODE: External input turns on internal repetition rate generator. First pulse occurs after start of gate signal with time delay defined by delay controls. Last pulse is always completed regardless of phasing between end of gate and pulse output. Maximum repetition rate: 40 MHz.
MANUAL: Front-panel pushbutton generates gate signal equal to time it is held down.

EXTERNAL WIDTH: Each input pulse results in one output pulse of same width but with controllable pulse levels and transition times. In this mode, repetition-rate generator runs independently at selected rate, producing triggers independent of main output.
MANUAL: Pressing front-panel pushbutton switches output level for time equal to time that pushbutton is held down.

BURST MODE (optional): Preselected number of pulses generated in response to each input trigger or pushbutton actuation. Number of pulses: 0 to 9999. Maximum repetition rate: 40 MHz. Minimum time between bursts: 200 ns.

General

OPERATING TEMPERATURE RANGE: 0 to 55°C.

POWER: 100, 120, 220, or 240 V (+5%, −10%), 48 to 440 Hz, 180 VA max.

DIMENSIONS: 16¾ in. W x 5¾ in. H x 15 in. D (426 x 145 x 380 mm).

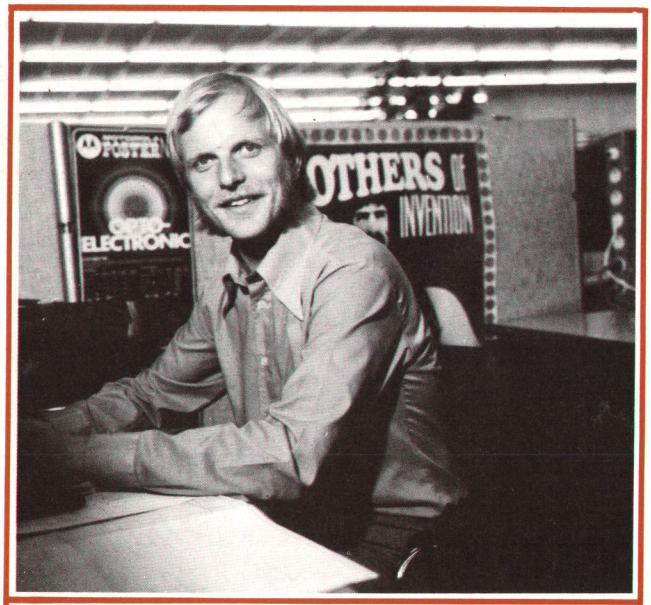
WEIGHT: 24¼ lbs. (11 kg).

PRICE IN U.S.A.: Model 8015A, $1750. Burst Option (002), add $350. Single output version (option 001), $1350.

MANUFACTURING DIVISION: Hewlett-Packard GmbH
Herrenberger Strasse 110
D-7030 Böblingen, Württemberg
Germany

MODE	SOURCE RESISTANCE*	LOAD IMPEDANCE	MINIMUM TRANSITION TIMES	PULSE LEVELS		PULSE AMPLITUDE		MAX REPETITION RATE
				UPPER	LOWER	MAX	MIN	
A sep B	50Ω 1 kΩ	50Ω 50Ω	<6 ns† <8 ns	+8 to −7 V +16 to −14 V	+7 to −8 V +14 to −16 V	8 V 16 V	1 V 2 V	50 MHz 40 MHz
	50Ω	>50Ω	<8 ns	Depends on load +320 to −280 mA max	Depends on load +280 to −320 mA max			40 MHz
A + B	50Ω 1 kΩ	50Ω 50Ω	<15 ns <15 ns	+16 to −14 V +16 to −12 V	+14 to −16 V +12 to −16 V	16 V 30 V	2 V 4 V	20 MHz 20 MHz
	1 kΩ	>50Ω	<15 ns	Depends on load +640 to −560 mA max	Depends on load +560 to −640 mA max			20 MHz

* Source capacitance = 30 pF. † At 8 V; may increase to 6.5 ns at 4 V.



Reinhard Falke

Graduating from Karlsruhe University (Germany) three years ago with a Diplom Ingenieur, Reinhard Falke went to work for Hewlett-Packard designing logarithmic amplifiers and rms-to-dB converters for real-time spectrum analyzers. A year later, he switched to pulse generators and then became Project Leader for the Model 8015A. For fun, he plays soccer with the HP GmbH Research and Development department's team, likes cars, and likes listening to contemporary popular music (known in the U.S. as rock-and-roll). He is married and has a two-year-old daughter and a three-month-old son.



Horst Link

Also a sometime member of the R and D soccer team, Horst Link spends his free time snorkel diving and taking photographs. Before joining Hewlett-Packard in 1970, he was with a firm making educational construction kits. Since being with HP, he contributed to the mechanical design of tape punches and tape readers for calculators and data acquisition systems before joining the 8015A team. He is married and has a 5-month-old daughter.

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